

Modeling of Large Scale RF-MEMS Circuits Using Efficient Time-Domain Techniques

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Abstract

RF-MEMS design is made difficult due to the lack of tools capable of simulating both MEMS devices and their surrounding circuits. Often MEMS components can have structures more than 100 times smaller than the surrounding circuit. This paper presents FDTD based techniques that can be used to simulate large structures containing finely detailed components. Particularly, a split-cell modeling technique is presented that allows for the modeling of a metal that intersects a cell. This technique is applied to the modeling of a MEMS capacitor. The technique allows for large cells to be used to model the entire device, with the split-cell modeling realizing the capacitor plate within a cell.

I. Introduction

RF-MEMS device design is a difficult and complex task. Many popular microwave design methodologies fail to provide accurate results for devices consisting of compound microwave circuits and MEMS devices. For example, microwave circuit simulators are limited by their models for various components, and cannot model all interactions between various (and physically disconnected) elements. As circuits become more highly integrated this limitation becomes increasingly apparent. Popular commercial electromagnetic simulators can compensate for these effects; however, their usefulness is limited by the size and complexity of the circuit that they can simulate. Often a hybrid approach is used wherein the electromagnetic simulator is used to model complex devices (such as MEMS), and the results are fed into a circuit simulator. This leads to simulation results that do not match measurement results of fabricated devices, which can lead to increased design times and a higher number of prototyping runs. The second major difficulty of this approach is the difficulty of modeling MEMS devices in several different configurations. By their very nature, MEMS are dynamic devices. To characterize a MEMS device through simulation, several states must be modeled. This adds to problem complexity by not only increasing the number of simulations that must be run, but in the number of configurations that must be created. Quite often, the time taken creating the simulation input and grid is a significant part of the simulation time. This paper presents variations that can be applied to the finite-difference time-domain (FDTD) electromagnetic modeling technique to model circuit elements that include MEMS devices. It then uses these techniques to model a MEMS capacitor.

One technique is the application of a variable grid [1]. A space-variable grid can be used to drastically reduce the number of cells needed to simulate a large problem. Small features can be accurately modeled, while features such as connecting lines can be represented efficiently. When applied correctly, this technique can provide an acceptably low level of dispersion.

The second feature that can be added to model these devices is subcell modeling. MEMS devices such as MEMS capacitors have membranes that can be very close to their supporting substrate. Using this spacing as a minimum cell size in FDTD can constrain the grid size for the entire simulation. By using a subcell modeling

technique to create a ‘split-cell’ intersected by a metal the grid is not limited by this small cell size. Furthermore, the split-cell method employed in this case can be used to place a metal membrane in an arbitrary location without modifying the remainder of the simulation. This provides two unique opportunities. The first is the ability to easily model devices in several configurations, the second is the ability to model dynamic devices by changing the metal position continuously during a simulation.

The following sections discuss these modeling techniques and present how they can be used to model an RF-MEMS capacitor. These techniques can be used to drastically reduce the computational resources needed to model a capacitor, allowing much larger overall structures to be simulated. These techniques are implemented in such a way that they can be easily added to an existing FDTD code.

II. Variable Gridding

One of the most constraining aspects of an FDTD simulation comes from the requirement that the cell width be equal to (or often smaller than) the smallest feature of the device being simulated. When simulating structures consisting of several different elements, such as MEMS circuits, this can lead to an extremely large grid. For example, if a MEMS capacitor that has a plate spacing of $3\mu\text{m}$ is situated on top of a $525\mu\text{m}$ substrate, 175 $3\mu\text{m}$ cells (using the coarsest representation possible) are needed compared to 21 that could be used with a $25\mu\text{m}$ spacing. If similar limitations occur in the other two dimensions of the grid, the total number of cells needed for the simulation can easily grow prohibitively large.

A subgridding method which can compensate for this problem has previously been presented [2-3]. This technique subdivides sections of the FDTD grid, creating finer grids in these areas. A routine must be implemented to interface the two different size grids. This is important because there are grid points in the refined mesh that do not exist in the coarse mesh. The mesh refinement used by this method is demonstrated in Figure 1a (in 2 dimensions).

The subgridding method is very useful for a variety of structures. In particular, this method can be used when small complex devices are embedded in a coarse grid, such as scattering problems or devices fed by microstrip lines. The difficulty in applying this method to an existing code comes from implementing the method by which the values in the subgrid are calculated. In addition, the method of determining these values usually requires that the subgrid be evenly spaced in the interior region.

Another method of modifying the grid to reduce the number of cells needed to simulate a structure is to introduce a nonuniform grid [4]. The nonuniform grid treats each direction separately, and allows each axis to be divided into any number of sections, each having a different cell length. The nonuniform grid technique is represented in 2D in Figure 1b. All three dimensions can be segmented in this way, creating a complex, and highly nonuniform, grid. This method can be applied to an existing code easily, dx , dy , and dz simply need to be changed

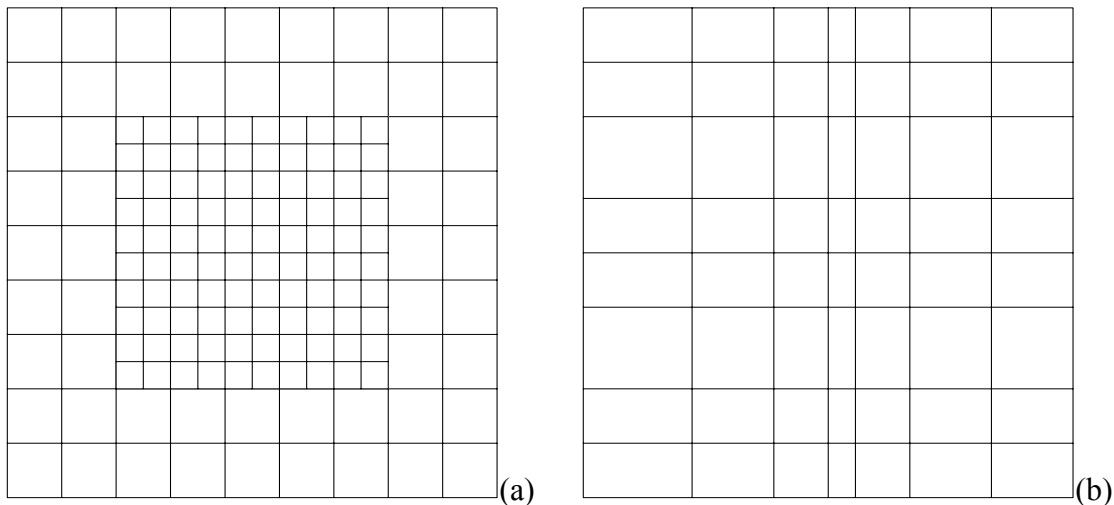


Figure 1: Variable gridding using (a) subcell and (b) nonuniform methods

from a constant to an array. In order to reduce ill effects that may rise from this method, it is important that the grid size not change from one cell to the next by more than a factor of two.

III. Subcell Modeling

The most difficult aspect of modeling RF-MEMS devices is the ratio between the feature size of the MEMS device and the feature size of the surrounding circuit. Often times feeding lines and matching networks can have features at least two orders of magnitude larger than the small MEMS devices. Using fixed, or even variable, FDTD grids to model these devices can lead to extremely large simulations. By reducing the need to use a fine grid, the number of cells needed to simulate a structure can be drastically reduced.

In addition to reducing the total number of cells required to simulate a structure there are other equally important advantages of using a split cell modeling method. This method naturally matches an important feature of MEMS devices, their reconfigurability. Using a fixed grid limits the number of states that can be modeled using FDTD to ones that can be placed on the fixed grid. In devices such as capacitors, small changes in plate position can have a drastic effect on their performance. Subcell modeling allows these features to be simulated in such a way that any position can be modeled. Thus, multiple configurations of dynamic devices and devices whose parameters change during simulation can be modeled.

The subcell method presented in this paper is based on techniques for conformal grid modeling [4] and subgridding [2]. The derivation presented is for a metal perpendicular to the y axis. This method has the advantages of being easy to integrate into an existing code and adding low computational overhead. This method could easily be extended to other directions and for curved structures that pass through cells.

Figure 2 shows a standard FDTD grid with a y normal metal intersecting two cells. Normally, metals are

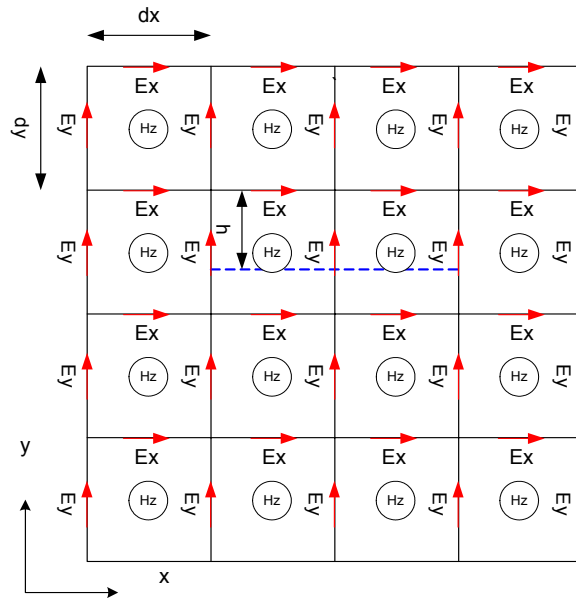


Figure 2: Metal intersecting FDTD grid

represented in FDTD by setting E fields tangential to the metal to zero. In the case presented in Figure 2 the grid could be regenerated to allow this metal to lie along cells containing the E fields. The structure that is being simulated may, however, make this impossible or impractical. Another method is to zero the nearest fields to the metal. However, this method effectively moves the metal to the nearest grid location and may cause unacceptable changes to the structure. A third option is to split the cell into two cells that share the metal as an interface.

This localized split cell modeling is demonstrated in Figure 3. By splitting the cell the metal is now on a grid location where tangential E fields exist. This technique doubles the number of cells in the area with the metal, however it only adds three field values per cell. In the case shown in Figure 3, these are Ey, Hx and Hz fields. The other fields are all located on the metal interface, and are always zero. The modified FDTD grid fits the structure, however, special field update equations must be used in the area of the split cell.

The update equations for the split-cell region can easily be determined using the Faraday's and Ampere's law in integral form derivation of FDTD [5]. Using this method the FDTD E field update equations are calculated using

$$\frac{\partial}{\partial t} \int_{S_1} \vec{D} \cdot d\vec{S}_1 = \oint_{C_1} \vec{H} \cdot d\vec{l}_1 \quad (1).$$

The contour used for this integration is taken from the Yee cell, as shown in Figure 4a. For the vast majority of the split cell region, standard update equations can be used with minor corrections. The Ey fields require no change. On the border regions, where the two grids meet, the same Hx and Hz fields are used to update the Ey fields above and below the split region. The domain of the H fields is the entire length of the cell, so no interpolation or averaging is needed. Slightly modified update equations must be used for the Hx and Hz fields in the split region. The dy value used in the updates must reflect the true length of the cell. In the area above the split, h (from Figure 3) and, in the lower area, dy-h must be used as dy. The H fields surrounding the split-cell region use the most heavily modified update equations.

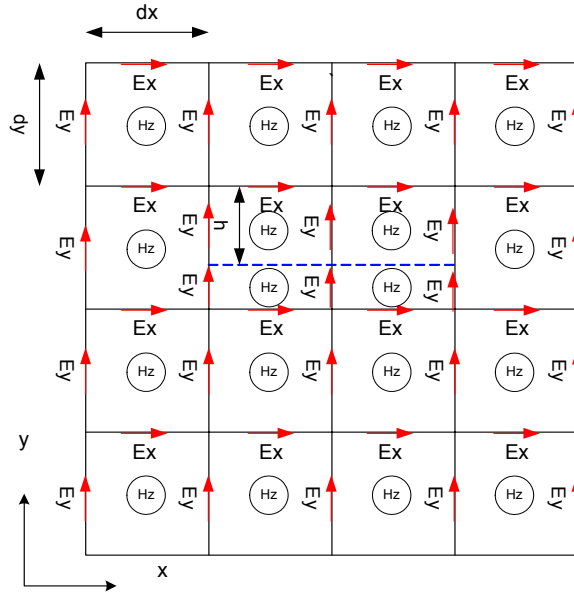


Figure 3: Metal intersecting subcell modified FDTD grid

The H fields bordering the split cell region have the Ey fields from both above and below the split metal in their Faraday contour. This is demonstrated in Figure 4 (b). The FDTD update equation for these fields uses both of the Ey fields, multiplied by their local dy. When determining the local update equations, careful consideration must be taken to correctly choose the fields used in the update. The Hz update equation used on the side of the split with the highest x value is

$$H_z \Big|_{i,j+1,k+\frac{\Delta x}{2}}^{n+1} = H_z \Big|_{i,j+1,k+\frac{\Delta x}{2}}^n + \left(\frac{\Delta t}{\mu} \right) \left[\frac{E_x \Big|_{i,j+\frac{\Delta x}{2},k+\frac{\Delta x}{2}}^{n+\frac{\Delta x}{2}} - E_x \Big|_{i,j+\frac{\Delta x}{2},k+\frac{\Delta x}{2}}^{n+\frac{\Delta x}{2}}}{\Delta y} - \frac{E_y \Big|_{i+\frac{\Delta x}{2},j+1,k+\frac{\Delta x}{2}}^{n+\frac{\Delta x}{2}} - \left(E_{y,above} \Big|_{i-\frac{\Delta x}{2},j+1,k+\frac{\Delta x}{2}}^{n+\frac{\Delta x}{2}} \cdot h + E_{y,below} \Big|_{i-\frac{\Delta x}{2},j+1,k+\frac{\Delta x}{2}}^{n+\frac{\Delta x}{2}} (\Delta y - h) \right)}{\Delta z} \right] \quad (2).$$

Similar equations are used on all sides of the split-cell region.

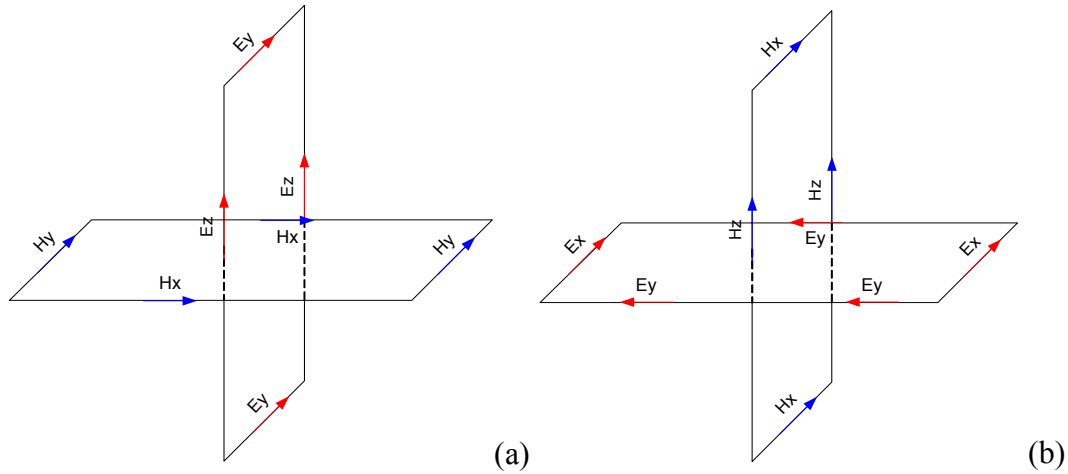


Figure 4: Orthogonal contours for determining update equations (a) standard (b) split cell border

IV. Example

The techniques discussed in this paper can be used to simulate large scale structures such as those found in modern MEMS circuits. These devices may use many MEMS elements in addition to a complex microwave circuit to connect the elements. These circuits may be large, necessitating the use of one or more of the above methods to simulate a device in a reasonable amount of time. One element that may appear in these circuits is a MEMS capacitive stub. These stubs can be used to provide a reconfigurable capacitance terminating a line. Several of these capacitors can be used in parallel to create a wider range of tunable values. These stubs are useful in reconfigurable circuits to create self-tuning systems.

One such stub is pictured in Figure 5. This stub uses a MEMS switch to connect to a large pad. The total capacitance of the stub is due to both the circuit and the pad. When the switch is in the up position, the capacitance is lower because there is no connection to the pad except for the relatively low capacitance of the switch in the “off” state, which adds in series with the capacitance of the pad. When the switch is in the down, or “on”, position, the capacitance is much higher due to the higher capacitance of the switch (nearly a short) and the pad in series.

Two simulations of this device were performed. The first simulation used the relatively mature variable grid method to accommodate the small capacitor spacing ($3\mu\text{m}$) and use a low number of cells to represent the $528\mu\text{m}$ thick substrate. For this simulation the smallest cell in direction of the thickness of the substrate is $3\mu\text{m}$, which transitions slowly to a $25\mu\text{m}$ spacing in the bulk of the substrate, and the air above. The grid in the other two directions is constant. The substrate for the MEMS device is silicon, with an ϵ_r of 11.7. The feed line is $130\mu\text{m}$ wide. The pad is $715\mu\text{m}$ wide and $880\mu\text{m}$ long. The gap between the feed line and the pad is $80\mu\text{m}$.

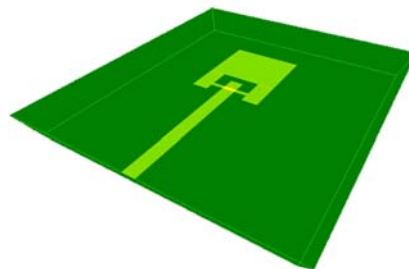


Figure 5: MEMS capacitive stub

The second simulation performed uses the split cell method. The split cell method uses a fixed grid in all dimensions. In the direction of the height of the substrate, the cell size is $24\mu\text{m}$. Using this spacing, the MEMS

switch exists $3\mu\text{m}$ from the edge of the cell. In order to provide a metal connection to the pad, the E_y fields at the x edges of the MEMS capacitor are zeroed.

The results of the simulation are presented in Figure 6. In addition to providing for more reuse of a grid for multiple circuit configurations, the split-cell modeling technique reduces the number of cells. The split cell grid is $86 \times 54 \times 77$, the variable cell grid is $86 \times 60 \times 77$. While this is not drastic, it would be very important in larger simulations, and could be more important if split cell modeling was used in multiple directions. Also, the total computational space was $1296\mu\text{m}$ long in the direction normal to the substrate in the split cell grid, versus $1151\mu\text{m}$

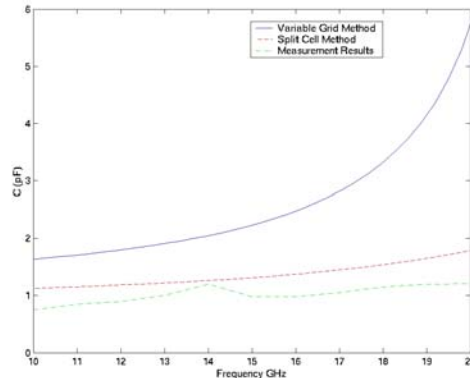


Figure 6: Capacitance of stub, variable grid, split-cell, and measurement

in the variable grid case. This demonstrates how fewer cells can be used to model a larger space. More importantly, the time step is several times larger in the split cell case due to the increased cell size. The split cell simulation required only 6000 time steps, compared to 30,000 for the variable grid.

It can be seen in this case that the split-cell simulation very closely matches the measurement results, while using relatively large cells. The variable grid used in this case scaled from $25\mu\text{m}$ cells to $3\mu\text{m}$ cells using intermediary cells approximately 1.5 times smaller than the previous cell. Seven different cell sizes were used to accomplish this. This was most likely too abrupt a change. In order to model the device more effectively, a more gradual change is required, which will result in a grid with many more cells.

V. Conclusion

MEMS circuits can be complicated to model using popular commercial tools. In particular, unexpected interactions that are not correctly handled by these tools can lead to a large amount of difference between simulated and measured results. This paper presents techniques that can be used to simulate these circuits using the FDTD technique. Specifically, a split-cell modeling technique was presented which allows the modeling of metals that cut through an FDTD cell. This method can reduce both the number of cells in a simulation and the number of time steps that a simulation must be run.

VI. References

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