

**Design of Experiments Technique for Microwave / Millimeter Wave**  
**Flip Chip Optimization**

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## **Abstract**

We present a design of experiments (DOE) technique for microwave/millimeter wave flip chip characterization and optimization. Two optimization approaches, signal bump misalignment and transmission line compensation, are combined together for optimal performance for high frequency operation. First, the design of experiments method is presented and its advantages are emphasized. Then, the two techniques are combined together in a factorial experiment with the purpose of optimizing the return loss to any desired frequency. The experiment is based on test structure fabrication and measurements. The one-factor-at-a-time strategy shows that return loss performance is increased with the misalignment values and decreased with compensation for the frequency range of interest. However, the statistical analysis revealed that the optimal performance is achieved for maximum compensation, and minimum misalignment. The optimal structure is measured from 1 to 75 GHz and shows return loss better than 17 dB. The method can be extended to include more optimization factors in different analysis intervals.

**Keywords:** RF/Wireless Packaging, Design of Experiments Technique (DOE), Flip-Chip

## 1 Introduction

Along with the recent advances in microwave and millimeter wave system development, the choice of interconnection solutions has become a very important issue, since their quality has a large impact on the performance of the entire system. For chip-to-package interconnection, the short electrical path provided by flip-chip [1] has made this solution the technology of choice for higher frequencies. With the increased interest in flip chip for higher and higher frequency applications, the optimization of the assembly performance to the millimeter wave region has become of great interest.

Previous work [2] shows flip-chip attached MMICs for a 76 GHz application where side via holes have been used to suppress radiation loss. The two factors considered for optimization in this paper are signal bump staggering [3] and compensation with a larger impedance transmission line section around the interconnection [4]. They are included in a factorial experiment based on test structure fabrication and measurements. The design of experiments approach has been applied successfully for flip chip design rule and scaleable lumped element model development [5], [6]. It provides the capability to quantify the effects of all factors involved in the optimization process and evaluate their joint interactions in any specified intervals of interest. Prediction of the assembly performance in those intervals can be performed based on the statistical analysis of the experiment outputs. Using the bump staggering and transmission line compensation as inputs, the optimization of the transition at 40 GHz is demonstrated. The optimal structure has been measured from 1 to 75 GHz and shows return loss better than 17 dB.

## 2 Design of experiments technique for design rule development

An experiment performed on a particular system gives the investigator the possibility to obtain objective and valid conclusions about the system. When developing design rules and optimizing the performance, a good understanding of all the issues involved is necessary. After recognizing and stating the problem, the experimenter has to choose the factors to be varied in the experiment, the ranges over which the factors will be varied and the specific levels at which the runs will be made. Then the response variable is chosen, making sure that it is relevant for the process under study, followed by the choice of the experimental design. For the purpose of design rule development and optimization, the simple  $2^k$  factorial designs [7] are recommended. They are widely used in experiments where it is necessary to study the joint effect of the factors on a response. They involve  $k$  factors, each at only two levels, therefore the response is assumed to be approximately linear over the range of the factor levels chosen. After choosing the experiment, the following steps include performing the experiment, the statistical analysis of the data and the conclusions and recommendations. For the factorial design, it is important to mention that all the conclusions are valid only within the specified intervals for the input variables. Generally, a successful experiment requires knowledge of the important factors, the ranges over which they should be varied, the appropriate number of levels and the proper units of measurements for these variables. The answers to these questions may come as the experiment evolves and some input variables are dropped, region of exploration for some factors is changed or new response variables are added.

The main advantages of this approach compared to other optimization techniques is that it gives a general understanding of how factors affect performance and how they interact and quantifies the effects in such a way that the designer can modify the most significant ones if the design process

resources are limited. The approach is also very flexible and different factors and intervals can be used as inputs for getting new conclusions on the system behavior.

To derive the equivalent circuit model, the variation of the physical attributes of the system has to be reflected in the values of the elements of the circuit. Regression models can be applied to the lumped elements in the model and a comprehensive and fully scaleable lumped element model including all the needed factors can be developed, as shown in [6].

This paper illustrates the application of a factorial experiment to the optimization of a flip chip interconnection to 75 GHz. Two known optimization techniques are combined together in a factorial experiment. There are three replicates for each treatment combination [7] and the output variables are the measured S-parameters.

### 3 Millimeter wave flip chip assembly optimization

#### 3.1 Variables

The first analysis includes the influence of the bump misalignment and transmission line compensation on the performance of the flip chip assembly. The analyzed configurations are presented in Figure 1. For CPW to CPW transition, the signal and the ground bumps have to be aligned for matching purposes. If the signal bump is purposely placed at a certain distance from the ground bumps as shown in Figure 1a, performance can improve [3]. This is due to the fact that reflection from the ground bumps does not add in phase, which leads to less reflection. The other optimization technique to be considered here is the compensation of the capacitive effect of the bump interconnection [4]. This is performed with a section of higher impedance transmission line around the transition, as shown in Figure 1b. First, the two optimization methods have been investigated separately. The signal bump misalignment values chosen are 1S, 2S, 4S and 8S, where  $S = 70 \mu\text{m}$  is the bump diameter, and the compensation  $\Delta G$  around the transition was chosen to be between 50 and 250  $\mu\text{m}$  in 50  $\mu\text{m}$  increments. The results of the preliminary simulations are presented in Figure 2. When each of the factors is varied independently of the other, it can be noted that the performance is improved in all the frequency band with misalignment and in the lower frequency band for the compensation. This would make us think that the optimal structure combining the two would include maximum misalignment and minimum compensation for frequencies higher than 30 GHz.

The next step is to combine the two techniques for optimal performance to 75 GHz in a factorial experiment. The two input variables are the signal misalignment ( $M$ ) and compensation ( $C$ ) and the values chosen for the two are, respectively, 0, 4S, 8S for  $M$ , and 100, 200 for  $C$ . The optimization

experiment is summarized in Table 1. Because of the very wide band analyzed, no systematic variation of the return loss has been observed. However, optimization can be performed at a specific frequency of interest.

### **3.2 Experiment**

The test articles were fabricated and measured. The substrate (2 inch x 2 inch) and die consisted of 10-mil-thick 99.6% alumina plated with 50 microinch gold over palladium on titanium tungsten. The plated substrate and die were photo-patterned and etched to realize the circuitry designed by Georgia Tech.

The die was attached to the substrate using a flip chip technique that employed gold stud bumps in tin solder to form the interconnection. Titanium bond windows were sputtered onto the die and substrates to act as targets for bump placement and solder dams to contain the solder during reflow, respectively. Stud bumps were bonded on the die in the interior of the windows using 1-mil diameter wire (99% gold, 1% palladium). On the substrate, tin was sputtered inside the windows to serve as bond pads for the corresponding die bumps. The die was then flipped and the bumps were aligned with the pads on the substrate. Finally, the entire assembly was reflowed at 350°C to form the flip chip interconnection.

A picture of the stud bump and a cross section of a resultant flip chip interconnection are shown in Figure 3. As can be seen in the figure, the stud bump was symmetric and uniform in shape. The solder wet the bump and the substrate plating completely without evidence of voiding, and the window was effective in containing the solder flow. The stand-off height of the interconnection measured approximately 40 microns.

As mentioned in the previous section, the multiple singularities in the frequency response make the design of experiments irrelevant for the entire frequency band. However, for a narrowband design systematic variation can be observed and the design of experiments method can be effectively applied for optimization.

For exemplification, the optimization experiment is performed for 40 GHz. The output variable is  $|S_{11}|$  and the sample size for the purposes of this experiment has been calculated to be 3 [7]. The values of the outputs are presented in Table 2. The data has been analyzed and the statistical significance of the two factors and their joint interaction is presented in Table 3.

The last column in Table 3 represents the F statistic for the two input variables and the two-factor interaction. F quantifies the statistical significance in the way that variables with higher F-values are more statistically significant. The threshold value for statistical significance has been calculated to be 3.2 for this application [7]. Every variable or interaction with an F value higher than 3.2 is considered to be statistically significant. As shown in the table, both variables are significant but the higher level of significance is the interaction between them. The optimal structure is run #2, zero misalignment and 200  $\mu\text{m}$  compensation. The one factor at a time analysis showed that performance is increased with the values of  $M$  and decreased with  $C$  for high frequencies, so the optimal structure would have been expected to be Run #5. However, the factorial strategy showed that the factors do not produce the same effect on the response at different levels of the other factor. Because of this very strong interaction, the optimal structure is found to be the maximum of compensation, and minimum of misalignment. For the specified analysis intervals for the two variables, this is proven to be the optimal solution.



The six structures have been measured from 1 to 75 GHz and optimal performance of better than 17dB to 75GHz has been recorded for Run #2, zero misalignment and 200  $\mu\text{m}$  compensation. The measurement result is presented in Figure 4.

## Conclusion

A design of experiments based technique for microwave/millimeter wave flip chip characterization and optimization has been presented. A full factorial design has been chosen to investigate two known optimization methods and combine them together in the optimal way at 40 GHz. The methods considered are signal bump misalignment ( $M$ ) and transmission line compensation around the flip chip transition ( $C$ ). Although individually the minimum compensation and maximum misalignment are optimal for frequencies higher than 30 GHz, it has been found that there is a strong interaction between these approaches and the optimal structure has maximum compensation (200  $\mu\text{m}$ ), but minimum misalignment (0  $\mu\text{m}$ ). This demonstrates that the DOE method gives a thorough understanding of the behavior of the flip chip assembly and a real optimization of the electrical performance over any desired frequency band can be achieved. The optimized structure has been measured from 1 to 75 GHz and it shows return loss better than 17 dB over the entire frequency band. By applying this to all the factors involved in the design process, the first comprehensive design rule set can be developed for any flip chip process at RF and microwave frequencies.

## **Acknowledgements**

The authors would like to thank Alan Boone at Rockwell Collins for developing the fabrication process and providing the test structures. Also, they would like to acknowledge the support of the Yamacraw Initiative of the State of Georgia, of the NSF Packaging Research Center of Georgia Tech and of the NSF CAREER Award No.9984761.

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<b>RUN #</b>	<b>MISALGNMENT (<math>\mu\text{m}</math>)</b>	<b>COMPENSATION (<math>\mu\text{m}</math>)</b>
<b>1</b>	0	100
<b>2</b>	0	200
<b>3</b>	4S	100
<b>4</b>	4S	200
<b>5</b>	8S	100
<b>6</b>	8S	200

Table 1. Treatment combinations

<b>RUN #</b>	<b><i>M</i> (<math>\mu\text{m}</math>)</b>	<b><i>C</i> (<math>\mu\text{m}</math>)</b>	<b><math> S_{11} </math> @ 40 GHz</b>			<b>TOTAL</b>
			<b>Replicate 1</b>	<b>Replicate 2</b>	<b>Replicate 3</b>	
<b>1</b>	0	100	-20.7	-19	-17.4	-57.1
<b>2</b>	0	200	-24.2	-31.3	-27	-82.5
<b>3</b>	4S	100	-16.2	-14.7	-15.1	-46
<b>4</b>	4S	200	-22.5	-22.8	-22.1	-67.4
<b>5</b>	8S	100	-20.2	-19.4	-18.5	-58.1
<b>6</b>	8S	200	-15.5	-15.5	-13.5	-44.5

Table 2. Optimization experiment for 50 GHz

<b>SOURCE</b>	<b>DF</b>	<b>SS</b>	<b>MS</b>	<b>F</b>
<b><i>M</i></b>	2	120.7	60.3	<b>19.8</b>
<b><i>C</i></b>	1	61.2	61.2	<b>20.1</b>
<b><i>MC</i></b>	2	153.4	76.7	<b>25.1</b>
<b>Error</b>	12	36.6	1.6	
<b>Total</b>	17			

Table 3. Statistical analysis for factorial experiment

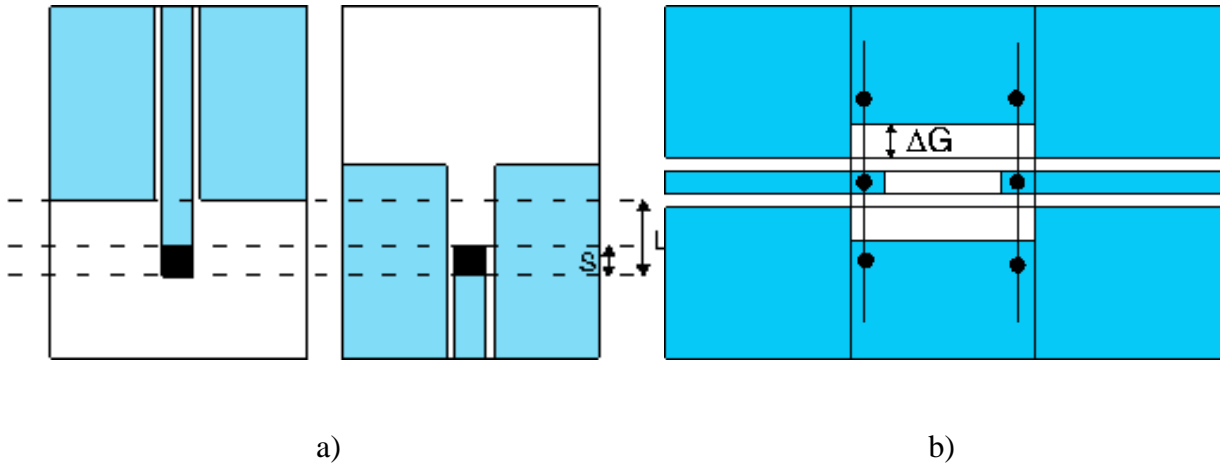


Figure 1. Analyzed configurations a) Misaligned signal bump b) Transmission line compensation

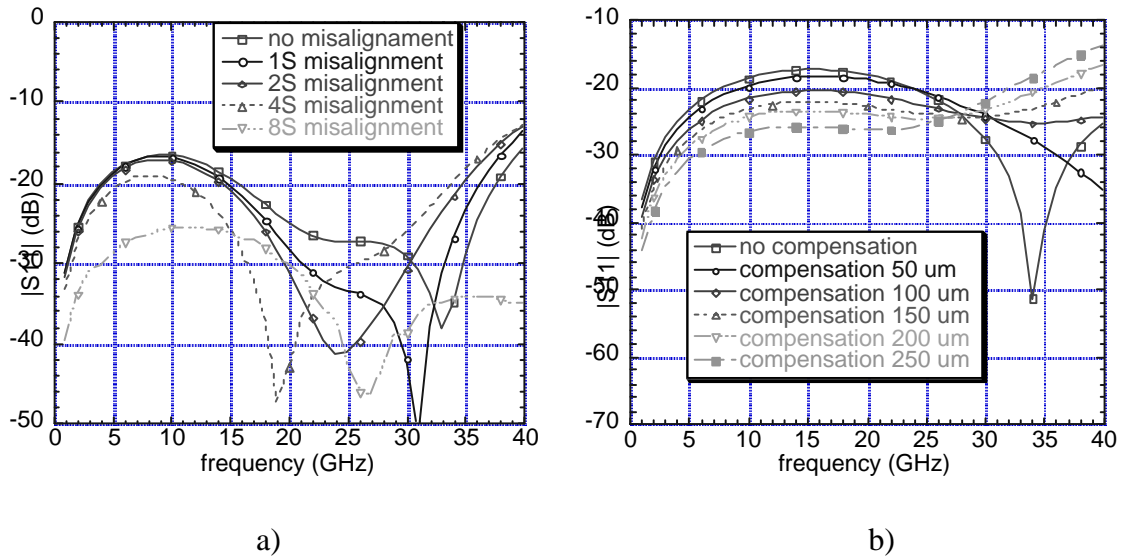


Figure 2. Simulation results for the optimization techniques a) Misaligned signal bump

b) Transmission line compensation

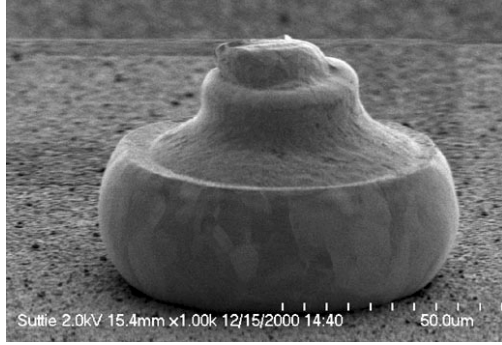


Figure 3. Stud bump before soldering

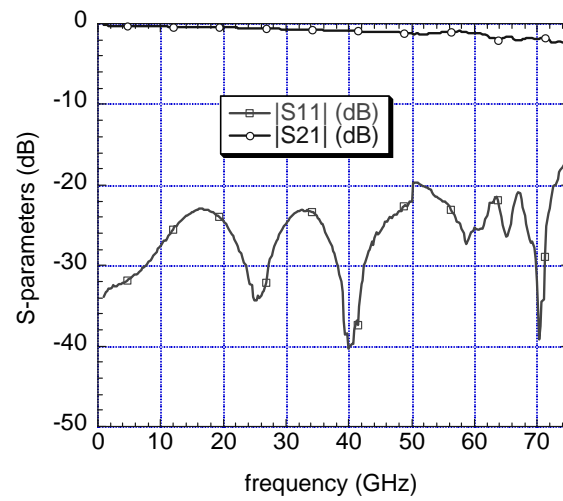


Figure 4. Measurement of optimized structure

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