RF Systems on Antenna (SoA): a Novel Integration Approach Enabled by Additive Manufacturing

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***Abstract*— This paper introduces for the first time, the novel concept of the system-on-antenna (SoA) which incorporates the ideas behind system-on-chip (SoC), system-on-package (SoP) and on-chip/package antennas, to create a new generation of fully integrated RF modules. This concept is only achievable using additive manufacturing, which is a rapid, on-demand and low cost fabrication technology. Instead of wasting valuable wafer or packaging area to create antennas, a novel method using 3D and inkjet-printing was utilized to embed a Ku-band radar module into a 10dBi horn antenna. The uniqueness of this system, lies in the fact that SoA topologies can be easily fabricated using additive manufacuturing, but unfeasible utilizing traditional fabrication techniques. This design methodology allows antennas to be compactly integrated within RF modules and sets the foundation for on-demand customizable SoA modules for a multitude of applications ranging from 5G+ and IoT to implanted medical and wearable applications.**

***Keywords*— Additive manufacturing, Inkjet printing, SoC/SoP, packaging**

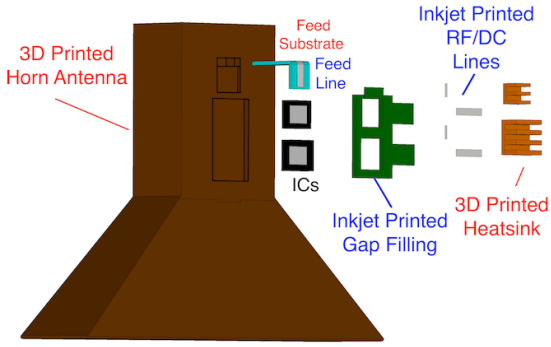
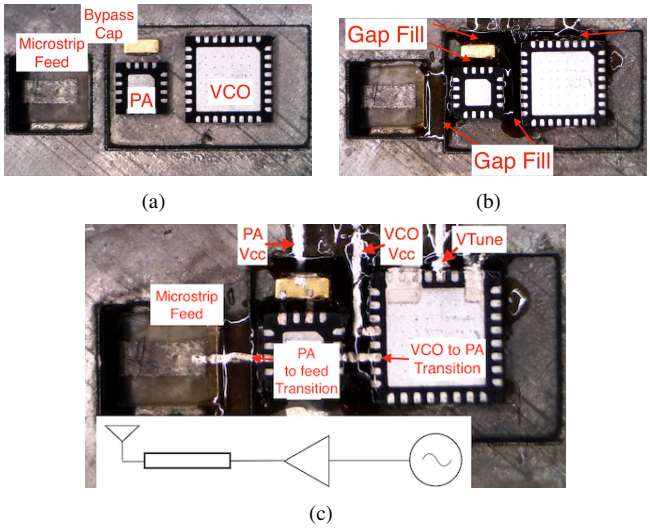


Fig. 1. Exploded view of the of a SoA proof-of-concept topology, demonstrating the many layers needed to be assembled. The ICs are an amplifier and VCO, with the amplifier amplifying the VCO signal to generate a wide range of signals based on the VCO tuning voltage. 3D parts are labeled in red, inkjet parts are in blue.

I. Introduction

Electronic systems are getting more and more complex and current trends for 5G and IoT demands require ever increasing levels of integration with higher performance targets at lower and lower cost. All of these factors led to the development of System-on-Chip (SoC) or System-on-Package (SoP), where entire systems are highly integrated onto a single microelectronic chip, or stacked together into a package. Recent works have also demonstrated integrated antennas on-chip or on-package. However, these antennas are usually very small, and consequently high frequency, since they need to be within the same order of magnitude as the size of a chip, so as to not use up valuable chip or packaging area. At higher frequencies, antennas need to have large gain values in order to overcome the path losses at these higher frequencies. Previous works such as [1],[2] and [3] demonstrates V-Band integrated on-chip/package antennas with low gain individual elements or array antennas. Due to the high frequency at V-Band, antennas need effectively 12-14 dB of additional gain to achieve the same link budgets at lower frequencies like Ku-band. To achieve 12-14 more gain requires adding multiple antennas into an array to achieve higher gain, or adding more power, both of which is not optimal or economically feasible. The cost of adding more amplifiers and multilayer feeding networks and the size increases of adding more antenna elements drastically reduces the feasibility of widespread integrated antennas.

In this paper, a novel way of compactly integrating systems and antennas is discussed, called System on Antenna (SoA), which leverages the flexibility of additive manufacturing, primarily 3D and inkjet printing. This fabrication process utilizes additive manufacturing to embed the IC active devices, the feeding lines and the heat management components onto custom 3D printed antennas. By combining the ideas behind SoC/SoP and 3D printed antennas, the SoA is created incorporating the benefits of high integration seen in SoC/SoP and on-chip/package antennas in a low-cost fashion, fabricated using customizable additive manufacturing techniques. Similar works have been explored in the analog/low frequency domain [4] using 3D printed electronics, but not yet in the RF domain. Others such as [5] and [6] have demonstrated many different examples of 3D printed horn antennas, however they do not shown any integration with any other devices or chips at the system level. By embedding chips within antenna, entire systems can be fabricated directly attached to the antenna, eliminating the need for flanges and coax transitions and cables which drastically reduces system size and loss. Additional size is minimized by eliminating the need for a PCB, since the electronic circuits are built directly on the antenna. This can only be achieved with additive manufacturing techniques, since the traditional chip/PCB fabrication methods are not suitable for structures such as horn antennas due to their inherent structural nonuniformities. The SoA makes use of valuable space on the antenna which would traditionally not have been utilized. Without loss of generality, the proof-of-concept application in this paper is a radar transmitter device which can be used for tracking applications. This requires a variable frequency source with



(a) (b)

(c)

Fig. 2. Fabrication of the chip attachment utilizing inkjet printing. (a) The chips, "L-shaped" microstrip output feed line and bypass capacitor for the PA are placed into the built-in cavity in the antenna. (b) SU8 gap filling. (c) RF and DC inkjet printed lines, with equivalent schematic.

frequency control. A Ku-band amplifier and voltage controlled oscillator (VCO) are embedded into a 3D printed horn antenna, connected and selectively metallized using inkjet printing to enable transmission of Ku band signals for radar.

II. SoA Fabrication Methodology

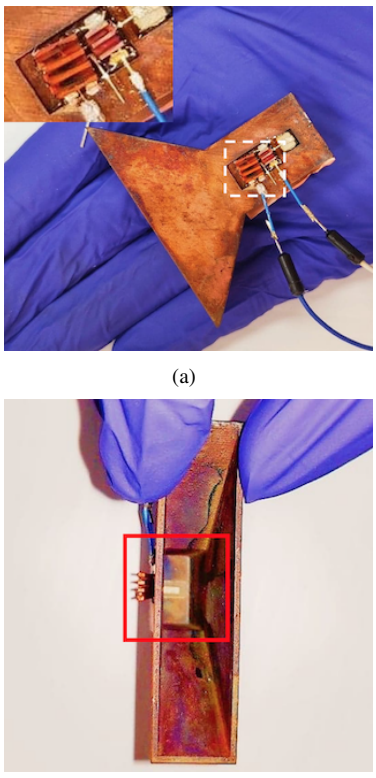
The fully additive manufacturing of the SoA module consists of four critical steps. 1) 3D printing and metallizing the antenna structure, with the built-in cavity IC housing. 2) Selectively metallizing the microstrip antenna feed. 3) Attaching chips and inkjet printing the gap fill and RF and DC interconnects between VCO, amplifier and antenna feed. 4) 3D printing the heat sink structure for heat dissipation. These fabrication steps can be seen in Fig. 1 which shows the assembly process, with everything except for the ICs, additively manufactured.

A. 3D Printed Antenna

The antenna chosen for this application is a Ku-Band pyramidal horn antenna, with an opening of 11.5 mm x 54 mm, attached to a standard WR62 waveguide section. This design is easily 3D printable on the stereolithography Formlab Form 2 printer with the High Temp Resin on $50\,\mu m$ layer resolution. The specialized High Temp Resin was used because of its heat deflection temperature of $239\,^{\circ}C$, which means that the structure of the antenna will not bend due to later sintering steps. Cavities were left on the surface of the waveguide section of the horn antenna to allow embedding of the RF chips and the microstrip feeding. The cavity was designed to be 1 mm deep (the thickness of the QFNs) so that the ICs lay flat with the surface of the antenna when placed within the cavity. The cavity was made wide (8 mm) to house all the ICs and the bypass capacitor, and have around 0.5mm margin on either side for printing of the dielectric gap fill, explained later. The entire horn antenna was metallized first using electroless plating and then electroplated.

The metallization of the antenna structure was realized by electroless deposition of copper by following the procedures described in [7] with modifications. Specifically, a water-based solution, which contained 0.19 M cupric sulfate (anhydrous) and 0.67M sodium potassium tartrate tetrahydrate, was prepared with its pH adjusted to 12.5 using an aqueous NaOH solution. Appropriate amount of formaldehyde (37% in water) was then added to the solution to reach a concentration of 220 mM. The surface sensitized and activated antenna structure was incubated in the resulting copper electroless bath for 30 min at room temperature with occasional agitation. The resulting thickness of electroless deposited copper was around $3\,\mu m$.

While the electroless plating provides a conductive seed layer of copper that is bonded to the surface molecules of the 3D printed polymer, an electroplating process enables the ability to grow additional copper in a rapid and uniform manner. A copper acetate solution was created from 6 % acidic acid and copper. The amp-hours per area can be used to approximate the thickness of the coating. To double the thickness of the metallization in a uniform manner, a 0.12 A/h over a surface area of 64.9 square centimeter surface to increase the thickness by $4.9\,\mu m$ and constant agitation was used for deposition to create a uniform coating [8].



(a)

(b)

Fig. 3. (a) The top view of the SoA module prototype with enlarged heat sink (inset). (b) Side view clearly showing the L-shaped microstrip feed inside the horn.

B. Microstrip Feeds

From previous literature discussing 3D printed horn antennas, the feed structure is rarely discussed, due to the difficulty in selectively metalizing the feeding structure. The feed structure needs to effectively connect the RF chips on the outside of the antenna to the inside of the waveguide to excite the antenna. Therefore, a microstrip probe feeding structure is designed in a "L-shaped" 3D printed piece with one side inkjet printed using EMD 5730 silver nanoparticle (SNP) ink to fashion a 50 Ωmicrostrip line. The microstrip feed is then sintered at 150 °C, and then individually inserted into the microstrip cavity designed into the antenna structure. The bent L-shaped microstrip feed lies compact and flush with the surface of the antenna and does not affect significantly the insertion loss or bandwidth compared to an equivalent coaxial probe feed.

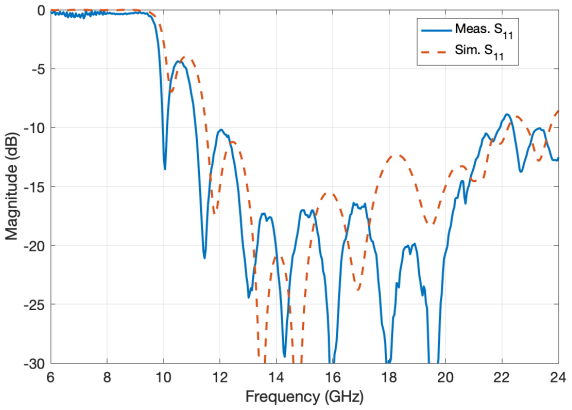
C. Chip Attachment/Interconnects

The radar transmitter device consists of a VCO (HMC632LP5E) and an amplifer (HMC451LP3), both QFN packaged devices. To attach the QFNs to the antenna, they are first flipped over and epoxied down into the built-in cavity in the antenna to expose the metallic pads. Due to the gaps that form in between the chips, the cavity walls and between the chip and microstrip feed, the space needs to be filled in with dielectric material, enabling the realization of inkjet-printed flat low-parasitics interconnecting electrical traces. The dielectric material used to fill the gaps is SU-8 ink (MicroChem) printed at 60 °C platten temperature. The gap filling is a major challenge due to the deep cavity that needs to be filled. Thus, the drop density was increased to 16000 DPI for rapid filling and required approximately 30 layers of Su-8 to totally fill to the edges of the chip. Su-8 underwent two UV cure cycles, once when the gap is half way filled and one where it was fully filled to ensure that the entire gap is fully UV cured. After fully UV curing and hardbaking of the SU-8, the Su-8 hardens allowing for further metallization of the surface using SNP, realizing the RF and DC connections. The process is demonstrated in Fig. 2 showing the step by step processes of connecting all the devices using inkjet printing.

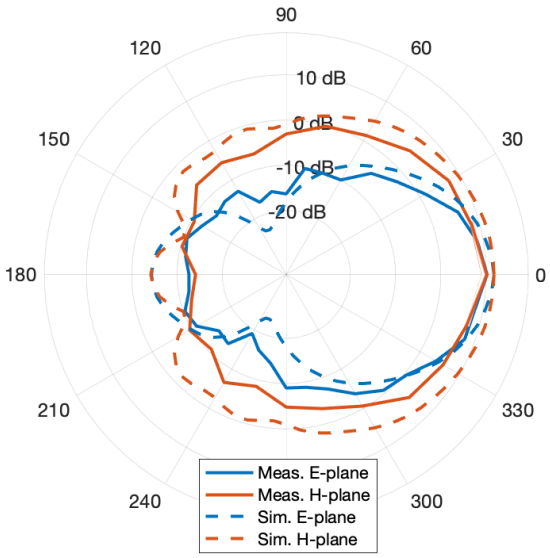
D. Heat Sink

Heat sinks are important devices used to dissipate heat to the environment. Low power chips like low-noise amplifiers and passive components typically do not require the use of heat sinks, but the HMC632LP5E and HMC451LP3 both consume around 1 W of power during operation, which necessitates the need for heat sinks. The fact that they are also flipped over with no PCB metal on the ground paddle, further exacerbates the need for heat dissipation. Prototypes that do not have the heatsinks attached, were only operational for seconds, before overheating damaged the device.

The heat sinks were 3D printed and electroplated in the same electroplating process explained above. The electroplating current and duration was increased to 50 mA and 4 hours respectively, to develop a thicker film of copper



(a)



(b)

Fig. 4. Simulated and measured horn antenna: (a) S11, and (b) gain pattern.

to allow better heat dissipation. The smaller dimensions of the amplifier, with only a footprint of 3 X 3 mm^2 provides the biggest challenge due to the small size. Regardless, the 3 fin, 3 X 3 X 4 mm^3 3D printed copper electroplated heat sink fabricated for the amplifier was calculated to be achieve 58 °C/W of thermal resistivity which is less than the 78 °C/W maximum rating for the chip, allowing the amplifier to be safely operated. A passivation layer of Su-8 was printed on the pads of the chips to prevent shorting. The heatsinks were attached using Arctic Silver thermal compound and the completed system with the assembled heatsink on top of the chips is shown in Fig. 3.

III. Measurements

Initially, the horn antenna was printed with a flange connection to verify its successful RF performance along with a satisfactory performance of the copper deposition. The input matching and gain patterns are both measured and matched with simulations closely. The gain of the antenna was measured to be 10 dBi which is only 0.5 dBi less than

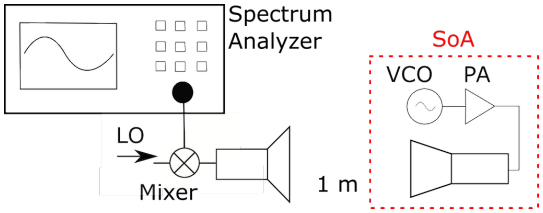


Fig. 5. Measurement setup of the SoA. The VCO on the SoA is externally adjusted to examine the frequency shifted response.

the simulated antenna, demonstrating that the 3D printing and copper plating process was a success and that the surface roughness of the 3D print did not have a large effect. These results are shown in Fig. 4.

However, it was difficult to measure the standalone microstrip fed horn antenna since there was no coaxial connection to the measurement equipment. Thus only empirical experiments were conducted for the SoA by turning on the SoA and altering the tuning voltage of the VCO to view the resulting frequency shift on a spectrum analyzer. A standard gain horn antenna was used as the receiver for the spectrum analyzer, and a mixer (ZX05-24MH-S+) was used to step down the frequency so it can be measured by the spectrum analyzer, shown in Fig. 5.

The frequency shifted data while the device was under operation is shown in Fig. 6. When the voltage of the VCO was changed from 7 to 9 volts, a frequency shift is observed in the spectrum analyzer, demonstrating that the device is operational, and the device can output a wide range of signals for potential radar applications. The received frequencies were 14.7GHz, 15GHz, and 15.26GHz for 7V, 8V and 9V tuning voltage of the VCO respectively, which were subsequently downconverted by mixing 13GHz. The received power level of the device is around -33.3 dBm for 9V Vtune and -33dBm for 7V Vtune. This translates to a total system loss of 2.5-2.8 dB. The amplifier was operated at maximum saturated power of 20 dBm at 15 GHz. The pathloss measured at the same distance using the reference 3D-printed flange antenna was -40.5 dB, and the mixer conversion loss is 10 dB at 2GHz IF. The expected received signal level, assuming everything to be lossless, is around -30.5 dBm (20 - 40.5 - 10 = -30.5). Thus, there is a loss of around 2.5-2.8 dB in the transition from the SoA to the antenna.

IV. Conclusion

In this paper the fundamental idea of SoA is explored, which provides the benefit of effectively integrating an RF system (such as SoC/SoP) with a complex antenna (such as on-chip/on-package antennas). The SoA provides a high level of integration with minimal losses, and the added benefit of being additively manufactured, greatly reduces the cost and time of realizing such a system. Future work includes integrating automated VCO control using microcontrollers and battery/energy harvester integration for fully standalone systems, and minimizing losses by optimizing the inkjet printed interconnect's shape and length.

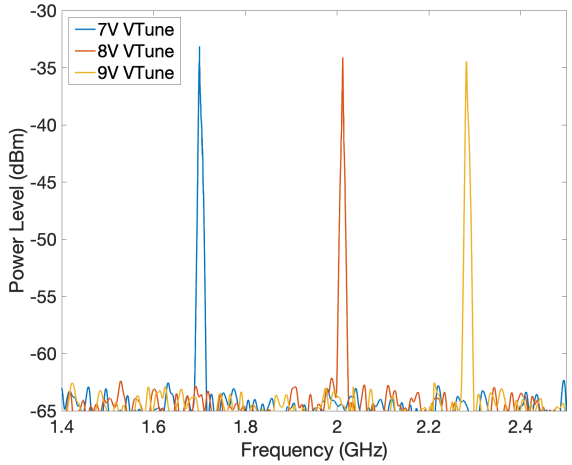


Fig. 6. Received power level from the SoA, with different tuning voltage. The frequency received is 14.7GHz, 15GHz, and 15.26GHz for 7V, 8V and 9V tuning voltage respectively. The frequency measured is post frequency conversion due to the mixer.

Additionally, optimizing the structure, such as stacking chips on top of each other can further miniaturize the SoA. This design methodology can be applied to many different applications such as dedicated amplifiers, or front-end module transceivers, which can be utilized in all manners of wireless communication. The benefits of utilizing these techniques outlined in this paper can help create scalable autonomous wireless systems that could drastically reduce the development cycles of new RF, 5G and IoT systems.

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