A New Contactless Assembly Method for Paper Substrate Antennas and UHF RFID Chips

Federico Alimenti, *Senior Member, IEEE*, Marco Virili, Giulia Orecchini, Paolo Mezzanotte, Valeria Palazzari, Manos M. Tentzeris, *Fellow, IEEE*, and Luca Roselli, *Senior Member, IEEE*

***Abstract*—This paper deals with a low-cost method for the assembly of flexible substrate antennas and UHF RF identification silicon (Si) chips. Such a method exploits a magnetic coupling mechanism, thus not requiring for galvanic contacts between the Si chip and antenna itself. The magnetic coupling is established by a planar transformer, the primary and secondary windings of which are implemented on flexible substrate and Si chip, respectively. As a result, the Si chip can be assembled on the antenna with a mere placing and gluing process. First, the idea has been validated by theory. Electromagnetic simulations of a square heterogeneous transformer (1.0-mm side) show a maximum available power gain (MAG) of −0.4 dB at 868 MHz. In addition, the heterogeneous transformer is also quite tolerant with respect to misalignment between primary and secondary. An offset error of 150 μm reduces the MAG to −0.5 dB. A sub-optimal matching strategy, exploiting a simple on-chip capacitor, is then developed for antennas with 50-Ω input impedances. Finally, the idea has been experimentally validated exploiting printed circuit board (PCB) prototypes. A PCB transformer (1.5-mm side) and a transformer rectifier (two-diode Dickson multiplier) have been fabricated and tested. Measurements indicates a MAG of −0.3 dB at 868 MHz for the transformer and the capability of the developed rectifier to supply a 220-kΩ load at 1.5 V with a −2-dBm input power.**

***Index Terms*—Flexible electronics, heterogeneous integration, ink-jet paper printed antennas, RF identification (RFID), RF transformers.**

I. Introduction

RF identification (RFID) tags working in the UHF frequency range rely on ultra-low power CMOS circuits and flexible substrate antennas [1]. Today, the typical cost of these tags is around $0.1, most of this amount being associated to the assembly of the CMOS die on the flexible substrate. Among several mounting processes, the most effective one [2] is based on fluidic self assembly (FSA). With FSA, specifically shaped semiconductor devices are suspended in liquid and flowed over a surface that has correspondingly shaped holes or receptors on it and into which the devices settle. The shapes of the devices and holes are designed so that the devices are easily self aligned into place. FSA is typically divided in six process steps, the last one being devoted to the electrical connection of the assembled CMOS chip via standard metallization techniques. Since the pads on the CMOS chips are relatively small in diameter (80 μm or less), an accurate alignment is required.

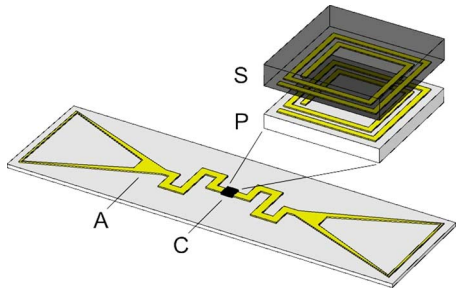

Fig. 1. RFID chip (C) is magnetically coupled to the antenna (A). Such a coupling is obtained by a transformer, the primary (P) and secondary (S) windings of which are fabricated on the antenna (paper) substrate and Si chip, respectively. In this way, the need for galvanic connection between antenna and chip is avoided. After [4].

In this paper, the possibility of completely avoiding the last FSA step (i.e., the electrical connection step) is considered. To this purpose, the CMOS chip is magnetically coupled to the antenna realized on the flexible substrate, thus eliminating all the galvanic contacts between the chip and the antenna itself [3], [4]. The magnetic coupling is established, as in Fig. 1, by a heterogeneous planar transformer, the primary and secondary windings of which are implemented on flexible (paper) substrate and Si chip, respectively. As a result, the RFID chip can be mounted on the flexible substrate by mere placing and gluing process steps. In particular, the chip will be padless and completely passivated, the pad-ring being substituted by the secondary coil (S in Fig. 1) of the transformer.

The first and more evident advantage of the novel design solution is the possibility to further reduce mounting costs by cutting one step of the FSA process. The second advantage is related to the market exploitation of flexible antennas on paper substrates [5]. These antennas can be fabricated by direct ink-jet printing, and thus, are well suited for ultra-low-cost RFID tags. The mounting of CMOS chips, however, has been never experimented, mainly because of the difficulty of establishing an electrical connection between the chip pads and the metal lines on paper substrate. That is exactly what the proposed solution eliminates.

Manuscript received March 12, 2010; revised July 27, 2010; accepted November 11, 2010. Date of publication January 31, 2011; date of current version March 16, 2011.

F. Alimenti, M. Virili, P. Mezzanotte, V. Palazzari, and L. Roselli are with the Department of Electronic and Information Engineering, University of Perugia, 06125 Perugia, Italy (e-mail: alimenti@diei.unipg.it).

G. Orecchini is with the Department of Electronic and Information Engineering, University of Perugia, 06125 Perugia, Italy, and also with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

M. M. Tentzeris is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

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Digital Object Identifier 10.1109/TMTT.2010.2103210

Flexible electronics, in fact, is facing a significant growth in terms of scientific attention and industrial investments due to the continuous request for light weight, shape adaptability, space saving, and economical, as well as environmental friendly electronics [6], [7]. This is leading the research toward the use of innovative technologies such as ink-jet printing on unusual substrates such as paper. Paper is recently showing to be more than a simple candidate for flexible RF electronics [5], [8]: it is a low-cost substrate since it is organic, and thus, universally available; it is well suited for reel-to-reel manufacturing and mass production. The ink-jet printing allows avoiding the commonly used etching process and it is a faster and cheaper technology with respect to the classical printed circuit board (PCB) manufacturing process (no photo-lithographic mask fabrication). Today, the most important fields of application of this innovative approach are RFIDs, wireless sensors, and flexible electronics [9], [10]. RFID tag planar antenna design has been already exploited as proof of the goodness of such a technological trend [11].

A first experiment of a tag antenna magnetically coupled to an RFID chip has been demonstrated in [3]. In [12], a UHF RFID tag has been realized on a standard 0.18-μm CMOS, including an on-chip loop antenna. In this paper, the two above ideas are further expanded. In particular, a multiturn primary winding is proposed in order to increase the coupling factor and to reduce the insertion losses. A further insertion loss reduction has been obtained by placing primary and secondary windings face-to-face. The heterogeneous transformer has been studied by means of electromagnetic simulations and the optimal solution to the matching problem is illustrated. An equivalent circuit is given and this can be used by the interested readers to test the impact of the magnetic coupling technique with already developed RFID tag designs. The placing errors in gluing the Si chip (with the secondary winding) on the paper substrate (with the primary winding) have been analyzed. Finally, the matching of a paper-antenna prototype has been studied and the experimental results have been obtained showing a transformer-coupled two-stage Dickson rectifier.

For the success of the proposed approach, two questions must be answered. The first question is related to the losses of heterogeneous transformer. The minimum losses are given by the maximum available gain (MAG) of the transformer itself, as suggested in [13], and can be achieved in simultaneous matching conditions. The second question concerns the interferences between the transformer magnetic field and the CMOS electronics. Such a point is particularly important when all the RFID tag circuitry is within the secondary winding of the transformer. In [14], however, it has been demonstrated that the above interference is negligible and that the "circuit-in-the-coil" approach is feasible.

This paper is organized as follows. In Section II, a paper to Si heterogeneous transformer is studied by means of electromagnetic numerical simulations. The MAG of such a transformer is taken as the main figure-of-merit and an equivalent circuit is derived. The effect of alignment errors is also considered in this section. Section III is devoted to the matching between the antenna and RFID chip. Starting from a fabricated and measured paper antenna prototype, both optimal and conventional strategies will be investigated. Finally, in Section IV, experimental results are presented. A PCB transformer and transformer–rectifier prototypes have been fabricated and measured to verify the feasibility of the idea and the accuracy of the design flow.

TABLE I
GEOMETRICAL PARAMETERS OF PAPER TO Si TRANSFORMER

Parameter	Primary	Secondary
material	paper	Si chip
number of turns	3	3
transformer side	1.0 mm	795 μm
track width	50 μm	10 μm
track spacing	50 μm	5 μm
track thickness	18 μm	3 μm
track σ	58 MS/m	58 MS/m
substrate height	260 μm	750 (Si bulk) μm
		3.7 (Epi layer) μm
		11 (SiO_2) μm
substrate ε_r	3.3	11.9 (Si bulk)
		11.9 (Epi layer)
		4.1 (SiO_2)
substrate $\tan\delta$	0.08	N.A.
substrate ρ	N.A.	50 (Si bulk) Ω cm
		20 (Epi layer) Ω cm

II. COUPLING TRANSFORMER

The proposed idea has first been validated by electromagnetic simulations. To this purpose, an heterogeneous transformer between the paper substrate and CMOS Si chip is studied. The geometry of such a transformer has been defined on the basis of the following constraints. On the paper substrate, the primary winding is assumed to be printed exploiting an ink-jet technology. The minimum metal track width and spacing are 50 μm, corresponding to the maximum spatial resolution of the ink-jet printer. On silicon, a typical RFID chip size of 1 mm^2 is considered. The secondary windings is substantially that reported in [12]. Such a winding could be substituted to the pad-ring of the chip and all the required tag electronics fabricated inside this coil. Further considerations on the heterogeneous transformer design are reported in Appendix A.

The complete parameter set is quoted in Table I. Primary and secondary windings have been placed face-to-face, as in Fig. 2, and separated by a distance of 50 μm. The spacing layer has been assumed filled of air ($\varepsilon_r = 1$). For the secondary coil, a 0.25-μm SiGe BiCMOS process has been taken into account. This process allows for five metal layers. The last two metal layers (top layers) are characterized by thick traces (i.e., 2 μm for M4 and 3 μm for M5), particularly suited for the fabrication of spiral inductors and transformers. The secondary winding has been implemented on M5.

The above structure has been numerically analyzed by means of a full-wave electromagnetic simulator. The obtained results are reported in Fig. 3 where the maximum available power gain (MAG) of the transformer is plotted. This figure-of-merit has already been used in [13] to characterize the coupling performances of integrated transformers. As can be seen form this figure, the MAG of the basic structure is -0.4 dB at 868 MHz, thus indicating that, with the right matching, only

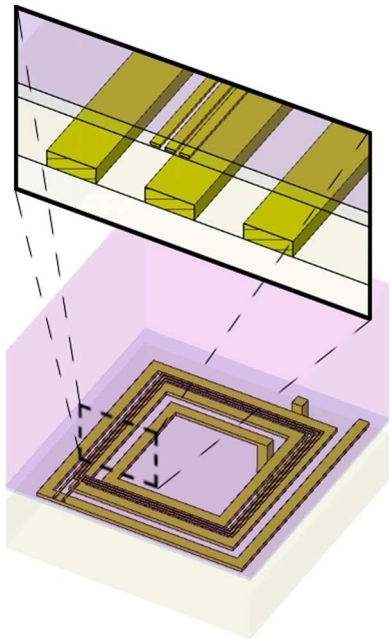

Fig. 2. Simulated heterogeneous transformer and zoomed cross section of the metal line geometry. Primary and secondary windings are designed to maximize the interfaced area under the given constraints.

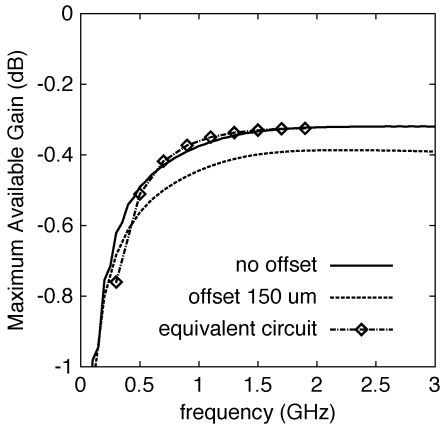

Fig. 3. MAG of the paper-substrate to Si chip transformer without and with alignment offset error between primary and secondary. The offset error is equal to 150 μm. The data obtained by electromagnetic simulations are compared to the MAG of the extracted transformer equivalent circuit.

8.8% of the incident power is lost inside the transformer (or, alternatively, 91.2% of the power is transferred from primary to secondary). The self resonance frequency of the structure is at about 3.5 GHz.

Now consider the case where a silver conductive ink is adopted for the printing of the primary winding. In this case, some of the parameters reported in Table I need to be adjusted. The silver ink conductivity, for example, is around 25 MS/m, as stated in [5]. The ink thickness, instead, is around 2 μm, as pointed-out by [15]. Repeating the above simulations with these values, only a minor degradation of the transformer MAG is observed, namely, from -0.4 to -0.5 dB at 868 MHz.

A second study that has been carried out is related to the effect of placing errors. These errors can arise when the RFID chip (carrying the secondary winding) is aligned with the antenna substrate (carrying the primary winding). At this point, it is important to recall that the FSA process is specified for an alignment error less than 1 μm and that bonding pads in CMOS chips do not have a diameter greater than 80 μm. In the proposed numerical experiment, an offset error as large as 150 μm is considered. With such an error, a galvanic contact down to 80-μm pads is no more feasible. With such an offset error, the MAG of the transformer is equal to -0.5 dB at 868 MHz, i.e., only -0.1 dB worse than that with perfect alignment (see Fig. 3). This means that the proposed innovation allows for automatic antenna-to-RFID assembly by standard pick-and-place machines, the latter being typically specified for a placing error of about 100 μm.

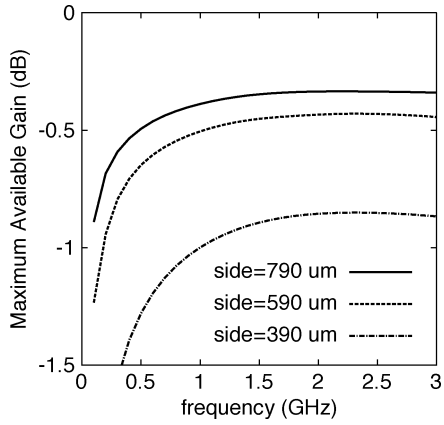

Fig. 4. MAG of the paper-substrate to Si chip transformer for different side lengths of the secondary (Si) winding. The size of the primary winding has been kept constant to the value of Table I.

Another parameter that has been considered during this study is the side length of the secondary (Si) winding. The RFID chip, in fact, has the trend of shrinking the size due to the continuous scaling of microelectronic technologies. As a consequence, the proposed magnetic coupling approach could have some limitations for very small RFID chips (i.e., secondary winding of small size). The size of the primary winding has been kept constant because this is mainly related to the resolution of the ink-jet printing process (see Appendix A). The results of such an analysis are reported in Fig. 4. From the figure, it emerges that the transformer with the smallest secondary winding (390 μm side) has a MAG of about -1 dB at 868 MHz. This value is only 0.6 dB worse than that of the typical case (790 μm side) in spite of a four times reduction of the active area.

Finally, the electromagnetic simulation results have been used to determine the parameters of a transformer equivalent circuit, according to the scheme of Fig. 5. This equivalent circuit has used by several authors to model Si integrated transformers [16], [17] and is available under Agilent ADS. The losses on the two substrates (displacement current on paper, displacement and eddy currents on Si) are modeled by the single resistor R_p. The equivalent circuit is derived in the frequency range from 300 MHz to 2 GHz (see Appendix B). The MAG of the extracted equivalent circuit is plotted again

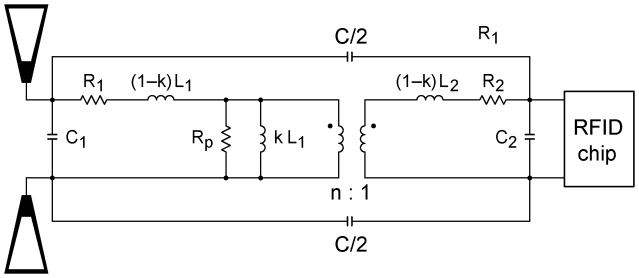

Fig. 5. Transformer equivalent circuit adopted to study the chip to antenna coupling. The paper to Si transformer parameters are $n = 0.711$; $k = 0.544$; $R_p = 2.7$ kΩ; $L_1 = 9.7$ nH; $R_1 = 0.3$ Ω; $C_1 = 55$ fF; $L_2 = 19.3$ nH; $R_2 = 5.2$ Ω; $C_2 = 65$ fF; and $C = 100$ fF. After [4].

in Fig. 3 and is in good agreement with the electromagnetic simulations.

III. Antenna to RFID Chip Matching

This section is devoted to the problem of the maximum power transfer between antenna and RFID chip, when the heterogeneous (paper-to-Si) transformer is exploited. As it is well known, passive, i.e., batteryless RFID tags, rely on the energy directly scavenged from the incoming RF carrier provided by the reader. Such an RF energy is rectified and used to supply all the tag electronics. Maximizing the power transfer through the heterogeneous transformer is thus a key design point to improve activation distance performances.

A. Simultaneous Conjugate Matching

For a lossy passive two-port network (which is a stable network by definition), it is always possible to find a pair of optimum source and load impedances, namely, $Z_S^{\rm opt}$ and $Z_L^{\rm opt}$, capable of maximizing the power transfer from input to output. In the case of the transformer geometry of Table I, these terminations can be visualized on the Smith chart, as in Fig. 6, along with the related constant gain circles.

From a design point of view, Fig. 6 indicates the optimum solution to the maximum power transfer problem. This means that, in order to let the transformer working in the best conditions as possible, the input impedances of both antenna and RFID circuit must be designed to meet $Z_S^{\rm opt}$ and $Z_L^{\rm opt}$, respectively, thus allowing the power transfer ratio from the antenna to the RFID circuit to achieve the MAG level of Fig. 3.

The above optimum terminations require a significant capacitive component, mainly because of the inductive nature of the transformer. The dipole antenna can easily be capacitively tuned working on its length (slightly shorter than the resonance length). The RFID circuit input impedance, instead, is mainly associated to that of its input stage, i.e., the rectifier stage. Such an impedance is naturally capacitive and can be tuned to the right value by means of a simple on-chip capacitor.

B. Paper Substrate Antennas

Antennas on paper substrates have recently been developed for ultra-low-cost UHF RFID applications [18]. These substrates are flexible, inexpensive, and characterized by a relatively good dielectric properties [5]. In addition, ink-jet

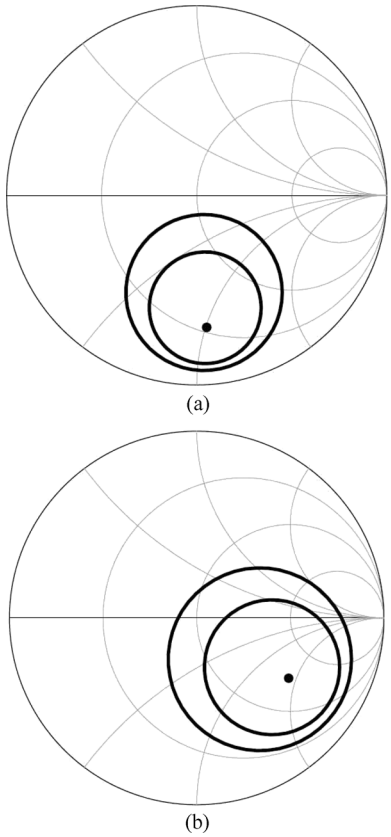

Fig. 6. Constant: (a) G_a and (b) G_p circles, with 0.25-dB gain steps, for the simulated paper to Si transformer. The MAG at 868 MHz is −0.4 dB for $Z_S^{\rm opt} = 18.5 - j50\ \Omega$ and $Z_L^{\rm opt} = 90 - j89\ \Omega$. After [4].

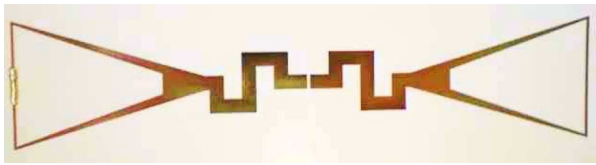

Fig. 7. Fabricated UHF bow-tie antenna on paper substrate. The overall dimensions are: length $l = 63$ mm and width $w = 27$ mm.

metal printing on paper was chosen as potentially capable of reel-to-reel manufacturing and mass production.

To further reduce costs, the well-known bow-tie antenna shape [19] has been modified in order to optimize the amount of silver ink used. In particular portions of solid printed surfaces have been removed, as shown in Fig. 7. A detailed study of such a design approach has been reported in [20] and will not be repeated here. This design is based on the current distribution of the bow-tie antenna. The highest concentration mainly occurs close to the center of the radiating body, and thus the related portion of metal is not removed. The simulated radiation gain is equal to 1.7 dBi.

The measurements have been performed using ground–signal (GS) probe tips with 1-mm pitch. The fabricated antenna was placed on a custom-made probe station (exploiting high density polystyrene foam with $\epsilon_r = 1.06$) to minimize backside reflections. The input reflection coefficient of the paper-substrate bow-tie antenna is shown in Fig. 8. The experimental data are in good agreement with electromagnetic simulations. The antenna

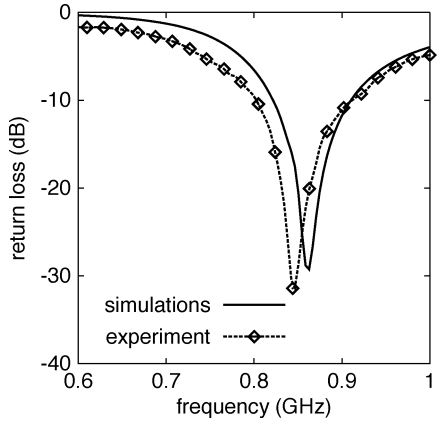

Fig. 8. Return loss of the fabricated bow-tie antenna: comparison between measurements and simulations. The structure is optimized for 50-Ω impedance matching within the 868-MHz frequency band. Data from [20].

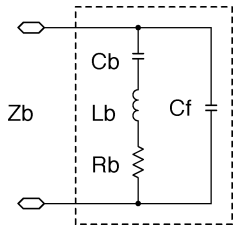

Fig. 9. Equivalent circuit of the bow-tie antenna input impedance. The circuit parameters are $R_b = 50\ \Omega$, $L_b = 64$ nH, $C_b = 0.54$ pF, and $C_f = 0.45$ pF.

exhibits a 7% bandwidth covering the European UHF RFID frequency range.

Finally, the bow-tie antenna input impedance has been approximated, in the considered frequency range, by the equivalent circuit shown in Fig. 9. This equivalent circuit is constituted by a series resonator R_b, L_b, and C_b (modeling the resonant behavior of the antenna itself) and by a parallel capacitance C_f. By inspection of Fig. 9, it is easy to obtain an expression for the antenna input impedance Z_b

$$Z_b = \frac{\left(1 - \frac{\omega^2}{\omega_b^2}\right) + j\frac{\omega}{\omega_b Q_b}}{-\frac{\omega^2 C_f}{\omega_b Q_b} + j\left[C_b + C_f + \left(1 - \frac{\omega^2}{\omega_b^2}\right)\right]} \tag{1}$$

where ω_b and Q_b are the resonance frequency and the quality factor of the antenna, respectively. These quantities are given by

$$\omega_b = \frac{1}{\sqrt{L_b C_b}} \tag{2}$$

$$Q_b = \frac{\omega_b L_b}{R_b} = \frac{1}{\omega_b C_b R_b}. \tag{3}$$

The equivalent-circuit parameters are quoted in the caption of Fig. 9 and have been found by fitting (1) to the measurements of Fig. 8. The agreement between the equivalent-circuit model and experiments is good, as illustrated in Fig. 10.

The bow-tie antenna of Fig. 7 is a typical example of a UHF RFID antenna, pre-matched at an impedance level of 50 Ω. A capacitive tuning of this antenna can be obtained adjusting the length of the folded line and the size of the radiating elements.

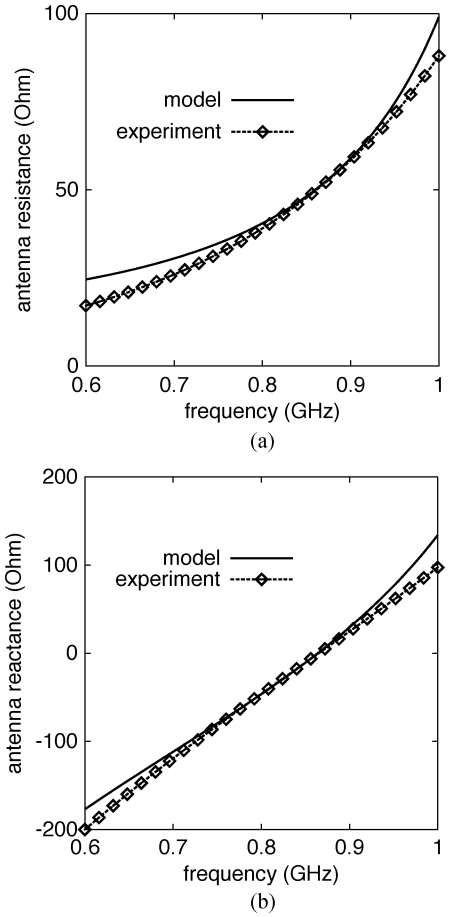

Fig. 10. (a) Real and (b) imaginary parts of the bow-tie antenna input impedance versus the frequency. Comparison between measured data and equivalent-circuit model.

C. Matching With On-Chip Capacitor

A sub-optimal solution to the maximum power transfer problem can also be found when an antenna, pre-matched to a 50-Ω impedance level, is given. In that case, one can only tune the RFID input impedance to a proper value. This situation is summarized in Fig. 11(a) where an on-chip capacitor C_m is adopted as tuning element. As a first-order approximation, it will be assumed that the RFID chip input impedance is purely resistive and equal to R_c. In practice, the impedance will mainly be determined by the rectifier circuit (as a function of frequency and input power) and it will have a capacitive value. In this study, such a capacitive value is embedded in C_m.

In order to evaluate the overall power transfer and to optimize it, the previously described bow-tie antenna is considered. This is a good example of pre-matched antenna with a 50-Ω impedance level at the frequency of 868 MHz. This study has been carried-out exploiting a Thevenin equivalent circuit for the bow-tie antenna in receiving mode, as depicted in Fig. 11(b). The Thevenin equivalent impedance is derived from the antenna measurements in transmitting mode and it has already been defined in Fig. 9. The open-circuit voltage $V_{\rm oc}$ is instead related to effective antenna area A_e and to the incident power density S_i (in watts per unit area) by

$$V_{\rm oc} = \sqrt{8 A_e S_i \eta \mathrm{Re}(Z_b)} \tag{4}$$

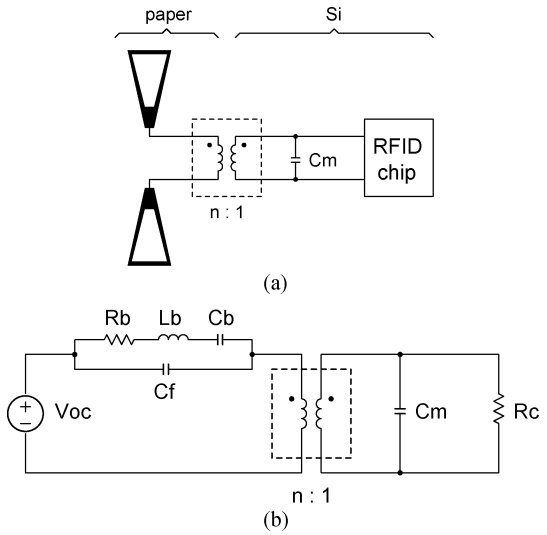

Fig. 11. Capacitor C_m can be used to optimize the power transfer between a pre-matched antenna (e.g., a 50-Ω antenna) and the Si chip. (a). To evaluate the overall insertion loss, a circuit model is adopted. (b). In this model, the bow-tie antenna is represented through a Thevenin equivalent circuit. The chip (mainly the rectifier input impedance) is described by the resistor R_c.

where η is the antenna efficiency and $\eta\mathrm{Re}(Z_b)$ represents the radiation resistance of the antenna.

The above Thevenin model has been connected to the primary winding of the heterogeneous transformer (see Fig. 5). The secondary winding, in turn, is connected to a capacitor C_m and to a resistor R_c, representing the on-chip capacitor and the rectifier stage input impedance, respectively. Finally, the overall power transfer has been evaluated, by a circuit simulator, as the parameter S_{21} between two terminations at different impedance levels, namely, Z_b for the input port (antenna side) and R_c for the output port (rectifier side).

The results of this study are reported in Fig. 12 for $C_m = 1.9$ pF and for three values of R_c. C_m has been tuned to maximize the overall power transfer at 868 MHz in the three cases. For $R_c = 350\ \Omega$, the overall power transfer is -1.5 dB (i.e., about 70%), a quite good value even for the suboptimal solution proposed. This resistance level can be tuned, during the design, by adjusting the number of stages of the voltage multiplier and the rectifier diode area [21]. In addition, part of the capacitance C_m is embedded in the rectifier input impedance.

IV. Experimental Results

As a proof-of-the-concept, a planar transformer and a transformer-rectifier (two-diode Dickson voltage multiplier) prototypes have been realized exploiting a standard PCB technology on an RO4003 substrate material. The proposed experiment is consistent with the concept to be proven since the typical resolution today achievable with metal ink-jet printing on paper is similar to that of the considered PCB technologies. As a consequence, transformer structures of similar dimensions and electrical performances can be fabricated and tested. In addition, the via-hole connection necessary to the transformer layout can easily be fabricated exploiting such a PCB process. Similar via-hole connections, although not yet fully optimized for paper substrates, have already been fabricated [22]: the typical via-hole diameter is 200 μm.

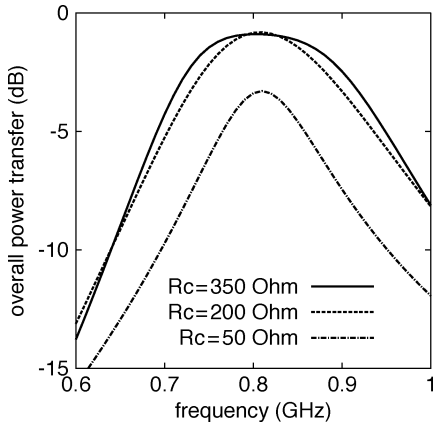

Fig. 12. Overall power transfer between bow-tie antenna and chip for $C_m = 1.9$ pF and three values of the chip input resistance R_c (mainly associated to the rectifier input resistance). For $R_c = 350\ \Omega$, an overall power transfer of -1.5 dB is obtained at the 868-MHz design frequency.

A. Transformer Results

To emulate the Si chip to paper substrate magnetic coupling, the fixture of Fig. 13 has been developed. Such a fixture is composed by two separated PCBs each of them with a three-turn winding. The outer terminal of the windings is fed by a 50-Ω microstrip line, while the inner one, is connected to the microstrip ground. Such a ground connection is provided by a via-hole at the center of the winding and by a short metal track printed on the same layer of the microstrip ground [see Fig. 13(b)]. In this way, it is possible to remove the microstrip ground from the winding active area, thus resembling the groundless structure of Fig. 1.

The geometrical parameters of the developed PCB transformer are quoted in Table II. Primary and secondary windings have been placed face-to-face, as in Fig. 13(a). In this case, the solder-resist film has been used to electrically isolate the two windings. The solder resist thickness is about 30 μm, whereas its relative permittivity is equal to 4. The two PCBs are equal, thus giving a symmetrical transformer whose windings have a side of only 1.5 mm.

The fabricated test-fixture is shown in Fig. 14. In particular, Fig. 14(a) illustrates one of the two PCBs with the small winding covered by solder resist and fed by the microstrip line. The complete transformer structure is shown in Fig. 14(b), where a second PCB is added on top of the first one and kept in position by four plastic screws (i.e., no glue is used here).

The structure of Fig. 14 has been experimentally characterized exploiting a vector network analyzer (VNA). The measured results are reported in Fig. 15 in a frequency range from dc to 1 GHz, i.e., including the RFID UHF 868- and 915-MHz bands. The discontinuities associated to both the SMA connector and to the feeding microstrip lines have been removed from measured data by means of a de-embedding procedure. This procedure is based on three steps. First, an open structure, i.e., a purposely designed calibration structure corresponding to Fig. 14(a) without the transformer coil, has been measured by the VNA. This open structure includes both the SMA adapter and feeding microstrip. A simple transmission line model of the open structure has then been assessed by fitting its computed S_{11} to that obtained by the calibration measurements. Finally,

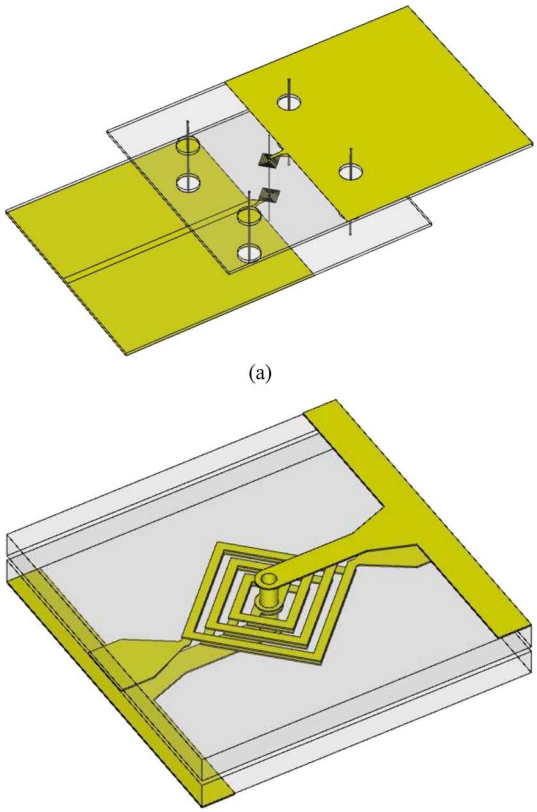

Fig. 13. Mechanical drawing of the: (a) PCB test-fixture and (b) zoom of its central zone with a highlight of the transformer structure. The tapering sections in (b) are used to connect the transformer to the feeding microstrips, whereas the two lateral bars are the related ground planes. From [4].

TABLE II
GEOMETRICAL PARAMETERS OF PCB TRANSFORMER

Parameter	Primary	Secondary
material	RO4003	RO4003
number of turns	3	3
transformer side	1.5 mm	1.5 mm
track width	100 μm	100 μm
track spacing	100 μm	100 μm
track thickness	17 μm	17 μm
track σ	58 MS/m	58 MS/m
substrate height	305 μm	305 μm
substrate ε_r	3.55	3.55
substrate $\tan\delta$	0.002	0.002

this transmission line model is used within a circuit simulator to extract the transformer scattering parameters.

The measured data have been compared to the electromagnetic simulations of the isolated transformer. As can be seen from Fig. 15, the overall agreement between measurements and simulations is good over the considered frequency range at 868 MHz$|S_{21}| = -3.3$ dB. This performance, however, is obtained in a 50-Ω measurement system. At the same frequency, the MAG (obtained from the measured scattering parameters) is much less and equal to only -0.3 dB. Due to symmetry, the simultaneous conjugate matching condition is given by $Z_S^{\rm opt} = Z_L^{\rm opt} = 55 - j63.6\ \Omega$.

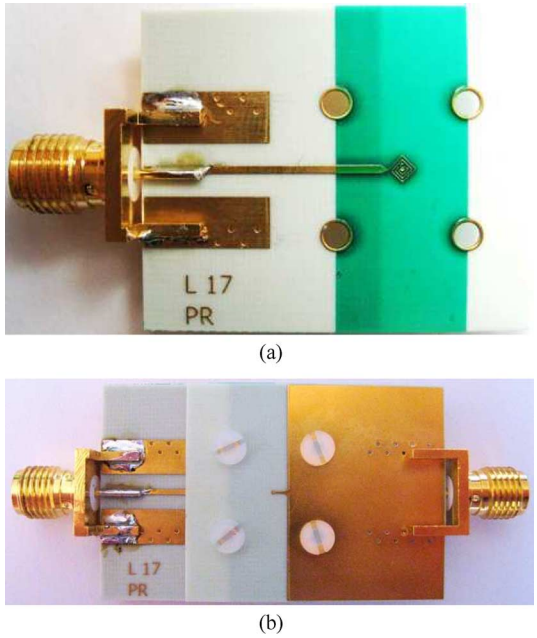

Fig. 14. Fabricated PCB test-fixture showing the: (a) primary winding alone and (b) the whole transformer. The latter has been obtained joining two equal planar windings in face-to-face configuration. From [4].

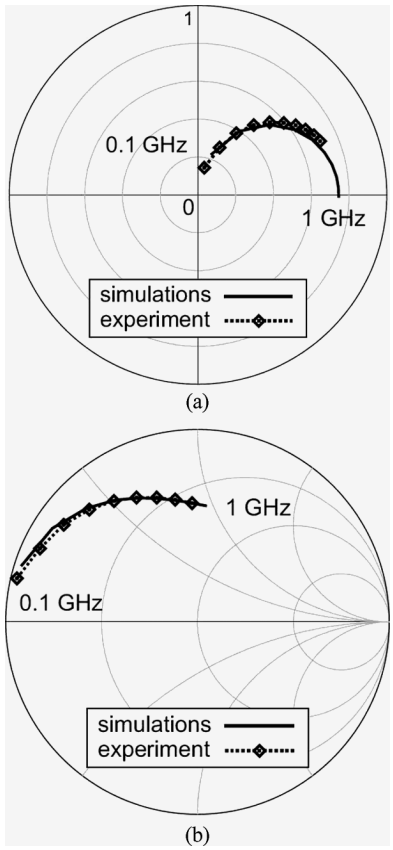

Fig. 15. Scattering parameters of the PCB transformer prototype: comparison between measurements and simulations. These data are referred to a termination impedance of 50 Ω at both ports. The MAG of this structure at 868 MHz is about -0.3 dB for $Z_S^{\rm opt} = Z_L^{\rm opt} = 55 - j63.6\ \Omega$.

B. Rectifier Results

The second test structure that has been verified is a transformer, the secondary winding of which is connected to a rec-

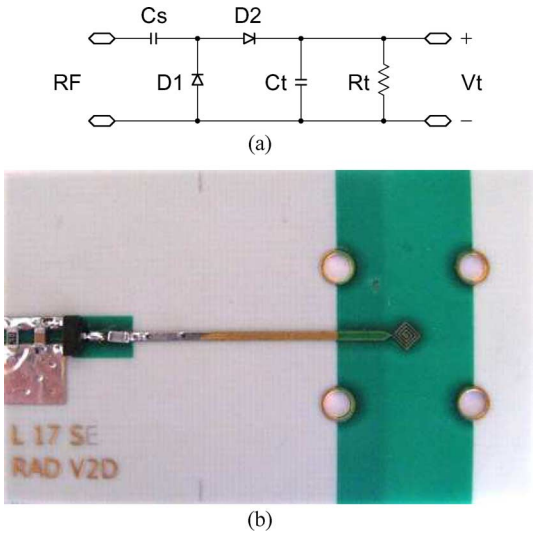

Fig. 16. Schematic of the: (a) two-diode Dickson rectifier and (b) fabricated PCB prototype. The two low-barrier Schottky diodes D1 and D2 are contained in the same package (HSMS2850 device). The values of the other components are $C_s = 20$ pF, $C_t = 1$ nF, and $R_t = 220$ kΩ.

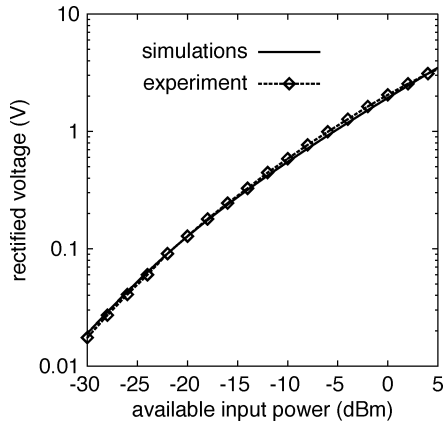

Fig. 17. Output voltage versus available input power for the transformer-rectifier PCB prototype: comparison between measurements and simulations. The data have been obtained at 868 MHz. An input power of -2 dBm is needed to supply at 1.5 V the 220-kΩ tag resistance.

tifier. In particular, the two-diode Dickson voltage multiplier configuration of Fig. 16(a) is adopted. The realized prototype is shown in Fig. 16(b) and it uses a matched pair of low-barrier Schottky diodes, i.e., the HSMS-2850 series device [23]. The power transmitted from the secondary winding output to the rectifier input has been optimized by properly tuning the length of the uniform microstrip line placed between these two circuits.

The characterization of the transformer-rectifier circuit has been carried-out in the following way. First, the PCB with the secondary winding and rectifier has been mounted on the top of another PCB where the primary winding is realized. As in the case of the transformer experiment, the two PCBs are kept in position by four plastic screws. The primary winding is then fed by an RF carrier at 868 MHz and the corresponding dc voltage is measured at the rectifier output. This experiment is repeated for several values of the available source input power and the results plotted in Fig. 17.

With the above experimental setup, a 220-kΩ load is supplied at 1.5 V when a -2 dBm is applied at the input. In these conditions, the dc power is 10 μW, this being a typical value for most RFID circuits.

At the same time, a numerical model of the whole transformer-rectifier structure has been developed. First an electromagnetic simulation of the transformer and of the microstrip line is carried out. The scattering matrix of such a circuit has then been inserted, as a black box, within a circuit simulator. Finally, the Dickson voltage multiplier has been analyzed with the harmonic balance (HB) tool.

The data obtained by the above co-simulation are reported again in Fig. 17 and they are in a very good agreement with respect to measurements. As a consequence, it is possible to conclude that the proposed coupling solution is working well and that the proposed design flow (i.e., electromagnetic simulation of the transformer and HB analysis of the rectifier) is accurate.

V. Conclusions

This paper has shown that a small RFID Si chip and large paper substrate, UHF antennas, can be efficiently coupled by means of a heterogeneous planar transformer. Primary and secondary windings of such a transformer are implemented on the paper substrate and Si chip, respectively. As a result, the Si chip will be completely padless, while a mere placing and gluing process will be required to assembly the whole RFID tag (i.e., antenna and Si chip together). The MAG of a 1-mm^2 heterogeneous transformer is in the order of -0.4 dB at 868 MHz, as obtained from electromagnetic simulations. In addition, such a transformer is quite tolerant to misalignments: a placing error of 150 μm reduces the MAG to -0.5 dB, i.e., only 0.1 dB worse than for a perfect alignment. It is worth noticing that a similar placing error is completely unacceptable in the case of standard galvanic contacts, e.g., for 80-μm diameter pads. As a consequence, a lower cost assembly process can be used exploiting standard pick-and-place tools, the latter already available in most PCB factories.

The maximum power transfer problem has been studied proposing both optimal (simultaneous conjugate impedances) and suboptimal (pre-matched antennas with 50-Ω input impedances) solutions. In the suboptimal case, only a simple on-chip capacitor and a proper rectifier input resistance are required. Finally, the above idea has been experimentally validated exploiting PCB prototypes. A PCB transformer (1.5-mm side) and transformer rectifier (two-diode Dickson voltage multiplier) have been fabricated and tested. The measurements confirm the feasibility of the proposed approach and the accuracy of the established design flow.

Exploiting the proposed design solution, the costs associated to the assembly of RFID tags could be reduced and novel technologies, such as paper antennas fabricated by means of ink-jet printing, enabled at market level.

Appendix A
Heterogeneous Transformer Design Criteria

The heterogeneous transformer described throughout this paper is composed by a square primary and secondary windings. The winding geometry is illustrated in Fig. 18 where w_i is the metal track width, s_i is the track spacing, $d_{\text{in}}^{(i)}$ is the

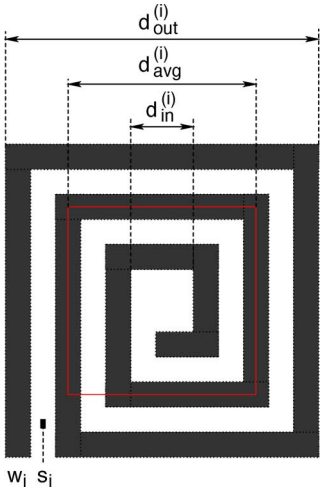

Fig. 18. Winding geometry and main parameter definition.

internal side length, and $d_{\rm out}^{(i)}$ is the external side length. In this formalism, $i = p$ stands for primary, whereas $i = s$ stands for secondary. Given a certain number of turns N_i, the external side length can be expressed as

$$d_{\rm out}^{(i)} = d_{\rm in}^{(i)} + 2N_i w_i + 2(N_i - 1)s_i. \tag{5}$$

The primary winding is realized on a paper, or more in general, on a flexible substrate. A central via-hole is needed to underpass the coil and to connect one of the two antenna terminals. The minimum diameter of such a via-hole on a flexible substrate is about 150 μm. In addition, a pad of at least 250-μm side is required to fabricate the metallized hole. This means that $d_{\rm in}^{(p)} \geq 250$ μm, thus setting a first constraint.

A second geometrical constraint is associated to the minimum track width and track spacing that can be realized with a given process. Typical ink-jet or photo-lithographic PCB feature resolutions are $w_p = s_p \geq 50 \div 100$ μm.

The secondary winding is realized on silicon. In this case, the feature resolution is that of the adopted technology node and does not imposes serious constraints to the coil layouts. The tag, however, has a certain size (typically in the order of one square millimeter) and the secondary windings should not waste additional silicon area. A good solution for the secondary geometry is obtained by replacing the pad-ring with the coil, while keeping all the electronic inside. A third geometrical constraint is thus imposed on $d_{\rm out}^{(s)}$ that should be less or equal to the tag side length.

As a consequence of the above considerations, we can conclude that the heterogeneous transformer has an asymmetric geometry and that, due to process resolution on paper or flexible substrates, the primary is larger than the secondary. In order to maximize the coupling coefficient, primary and secondary windings have been designed in such a way as to have the same average side length, i.e., $d_{\rm avg}^{(p)} = d_{\rm avg}^{(s)}$, where

$$d_{\rm avg}^{(i)} = \frac{d_{\rm out}^{(i)} + d_{\rm in}^{(i)}}{2}. \tag{6}$$

The design criteria is validated studying two variations of the structure in Table I. In the first one, the primary winding metal track width and metal spacing has been increased from 50 to 100 μm. In the second one, the secondary winding metal track width has been increased from 10 to 30 μm, keeping the 5-μm spacing. In all the cases, the same average side length $d_{\rm avg}^{(p)} = d_{\rm avg}^{(s)} = 750$ μm has been adopted.

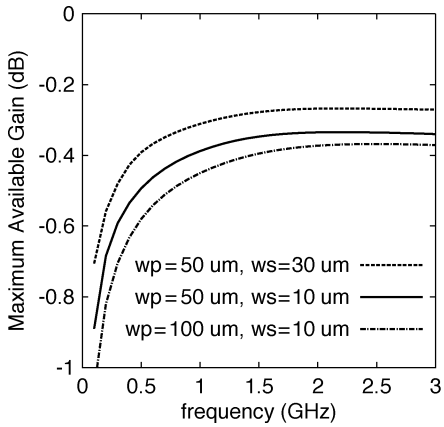

Fig. 19. MAG of the heterogeneous transformer versus the frequency for various primary w_p and secondary w_s metal track widths. In all the cases, the same average side length $d_{\rm avg}^{(p)} = d_{\rm avg}^{(s)} = 750$ μm is adopted.

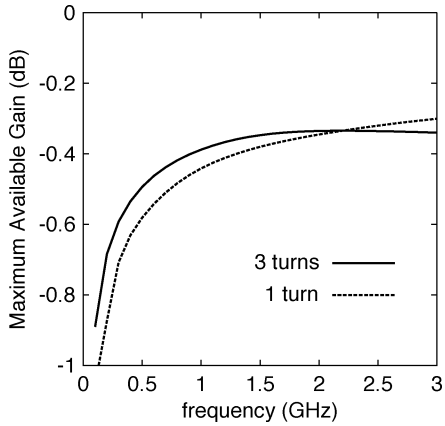

Fig. 20. MAG of the heterogeneous transformer versus the number of turns of the primary coil. The secondary coil has been kept constant, as in Table I. The three- and single-turn primary coils have the same average side length $d_{\rm avg}^{(p)} = 750$ μm.

The MAG of each structure is computed by electromagnetic simulations, and in Fig. 19, is compared with that of the basic structure ($w_p = 50$ μm, $w_s = 10$ μm). As can be seen, the obtained values are all within 0.2 dB. The best result is associated to the transformer with larger secondary track width, which is because of lower series resistance. The primary winding with lower feature resolution ($w_p = s_p = 100$ μm, i.e 100% worst than the basic case) reduces the transformer MAG of only 0.05 dB.

Another design criteria that has been evaluated is the number of turns of the primary coil. To study this effect, the structure of Table I has been compared with a transformer having the same secondary coil and a single-turn primary winding [3]. The single-turn primary winding is designed in such a way as to have the same average side length of that with three turns, i.e., $d_{\rm avg}^{(p)} = 750$ μm. The MAG of the two structures is reported in Fig. 20, and as can be seen, the transformer with the three-turn primary performs better than that with the single-turn primary. In particular, at the frequency of 868 MHz, the MAG values

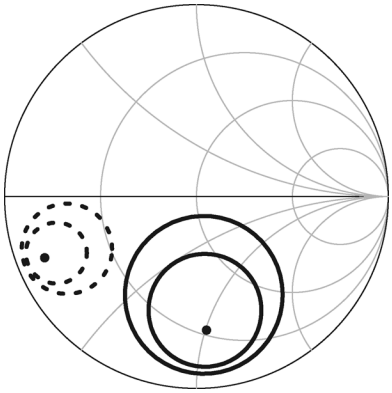

Fig. 21. Constant G_a circles, with 0.25-dB gain steps, for the simulated heterogeneous transformer with three- (solid line) and single-turn (dashed line) primary coil. In the case of single-turn primary, the MAG at 868 MHz is -0.46 dB for $Z_S^{\rm opt} = 4.1 - j9.6\ \Omega$.

are of about -0.4 dB and -0.5 dB for the three- and single-turn cases, respectively. Although the single-turn primary allows for single-metal layer ink-jet printing (no via-hole), the three-turn primary can be more easily matched to its optimum source impedance, as shown in Fig. 21.

APPENDIX B
TRANSFORMER EQUIVALENT-CIRCUIT EXTRACTION

The transformer equivalent circuit has been extracted from the electromagnetic simulations with the following procedure. First the computed scattering parameters of the structure are converted into impedance parameters. Primary and secondary inductances are evaluated with

$$L_1(f) = \frac{\Im\{Z_{11}\}}{2\pi f} \tag{7}$$

$$L_2(f) = \frac{\Im\{Z_{22}\}}{2\pi f} \tag{8}$$

where f is the analysis frequency. The coupling factor and the turn ration are given by

$$k(f) = \frac{\Im\{Z_{21}\}}{\sqrt{\Im\{Z_{11}\}\Im\{Z_{21}\}}} \tag{9}$$

$$n(f) = \sqrt{\frac{\Im\{Z_{11}\}}{\Im\{Z_{21}\}}}. \tag{10}$$

The series resistances are

$$R_1(f) = \Re\{Z_{11}\} \tag{11}$$

$$R_2(f) = \Re\{Z_{22}\}. \tag{12}$$

The equivalent-circuit parameters L_1, L_2, k, n, R_1, and R_2 have been obtained from the above functions for $f \to 0$. For example, $L_1 = L_1(0)$. C_1, C_2, C, and R_p have been determined by a best fitting in such a way as to recover the frequency dependence obtained with (7)–(12).

ACKNOWLEDGMENT

Agilent Technologies, Santa Clara, CA, and Computer Simulation Technologies, Darmstadt, Germany, are acknowledged for the EDA software licenses donation. G. Shaker, University of Waterloo, Waterloo, ON, Canada, is acknowledged for his support.

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Federico Alimenti (S'91–A'97–M'06–SM'09) was born in Foligno, Italy, in 1968. He received the Laurea degree (*magna cum laude*) and Ph.D. degree from the University of Perugia, Perugia, Italy, in 1993 and 1997. respectively, both in electronic engineering.

In 1993, he held an internship with Daimler-Benz Aerospace, Ulm, Germany. In 1996, he was a Visiting Scientist with the Technical University of Munich, Munich, Germany. Since 2001, he has been with the Department of Electronic and Information Engineering, University of Perugia, as a Research Associate, where he teaches classes on telecommunication electronics. In 2006, he was elected as a member of the Academic Senate of the University of Perugia. He has authored over 120 papers in referred journals, conference proceedings, and books chapters. His scientific interests concern the design and characterization of microwave integrated circuits in CMOS and SiGe BiCMOS technologies.

Dr. Alimenti was the recipient of the 1996 URSI Young Scientist Award.

Marco Virili was born in Terni, Italy, in 1983. He received the Laurea degree in electronic engineering from the University of Perugia, Perugia, Italy, in 2009.

Since 2010, he has been with the Department of Electronic and Information Engineering, University of Perugia, as an RF Designer. His scientific interests concern the electromagnetic modeling of buckles in waveguides and the design of low-power RFID systems.

Giulia Orecchini received the Laurea degree in electronic engineering from the University of Perugia, Perugia, Italy, in 2008, and is currently working toward the Ph.D. degree in electronic information engineering at the University of Perugia.

In Autumn 2008, she joined the ATHENA Research Group, Georgia Institute of Technology, Atlanta. Her research interests concern the development of RFID electronic systems and technologies.

Paolo Mezzanotte received the Ph.D. degree from the University of Perugia, Perugia, Italy, in 1997.

Since 1992, he has been involved with finite-difference time-domain (FDTD) analysis of microwave structures in cooperation with the Department of Electronic and Information Engineering, University of Perugia. Since January 2007, he has been an Associate Professor with the University of Perugia, where he teaches classes in microwaves and radio frequencies. He has authored or coauthored over 100 papers in international journals and conference proceedings. His research activities concern numerical methods, computer-aided design (CAD) techniques for passive microwave structures and analysis and design of microwave and millimeter-wave circuits. More recently, his interests have been mainly focused on the study of advanced technologies such as low-temperature co-fired ceramic (LTCC) and RF microelectromechanical systems (MEMS).

Dr. Mezzanotte is a reviewer for several IEEE publications.

Valeria Palazzari received the Laurea degree in electronic engineering and Ph.D. degree in information and electronic engineering from the University of Perugia, Perugia, Italy, in 2000 and 2003, respectively.

Since 2000, she has been with the High Frequency Electronics laboratory (HFElab), Department of Electronic and Information Engineering, University of Perugia. In Summer 2003, she joined the ATHENA Research Group, Georgia Institute of Technology, Atlanta. She is currently a Post-Doctoral Assistant teaching classes on telecommunication electronics. Her research interests range from the modeling, design, and realization of microwave integrated circuits in SiGe BiCMOS technology to packaging technologies for RF and wireless systems.

Manos M. Tentzeris (S'89–M'92–SM'03–F'10) received the Diploma degree in electrical and computer engineering (*magna cum laude*) from the National Technical University of Athens, Athens, Greece, and the M.S. and Ph.D. degrees in electrical engineering and computer science from The University of Michigan at Ann Arbor.

He is currently a Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta. He heads the ATHENA Research Group, Georgia Institute of Technology, which is comprised of approximately 20 researchers. He is the Georgia Electronic Design Center Associate Director for RFID sensors research, and he has been the Georgia Institute of Technology National Science Foundation (NSF) Packaging Research Center Associate Director for RF Research and the RF Alliance Leader (from 2003 to 2006). He has authored or coauthored over 320 papers in refereed journals and conference proceedings, three books, and 17 book chapters.

Dr. Tentzeris is a Distinguished Microwave Lecturer from 2010 to 2012. He was the recipient or corecipient of 14 awards, including the 2010 Uslenghi Best Paper Award.

Luca Roselli (M'93–SM'01) was born in Florence, Italy, in 1962. He received the Laurea degree in electronic engineering from the University of Florence, Florence, Italy, in 1988.

In 1992, he joined the Department of Electronic and Information Engineering, University of Perugia, Perugia, Italy, as a Researcher Associate. In 2000, he become an Associate Professor with the University of Perugia, where he teaches classes on microwave electronics, high-frequency electronic devices, and electronics fundamentals. He founded the WiS Srl and the DiES Srl, two University of Perugia spin-off companies. In 2008, he became Director of the Science and Technology Committee of the research center "Pischiello," Passignano sul Trasimeno, Perugia, Italy, for the development of automotive and communication technologies. He has authored over 160 papers in referred journals and conference proceedings. His scientific interests are the design of high-frequency electronic circuits, systems, and RFID sensors.