RF-System-On-Package (SOP) for Wireless Communications

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A new industrial revolution, often called the "third wave" or information technology (IT), is in the making. The products of this revolution will require entirely different systems hardware technologies: those with multifunctions, such as digital, analog, RF, and optical circuitries. RF and microwave design and packaging have been established as key technologies of this revolution. The demand for increasingly higher rates of data, voice, and video drives RF technology to ever higher frequencies where bandwidth for channel capacity is easy to find. Such emerging high-performance applications as personal communication networks, wireless local-area networks (WLAN), and RF-optical networks have defined a trend toward more flexible and reconfigurable systems. They impose very stringent specifications never before reached in term of low noise, high linearity, low power consumption, small size and weight, and low cost.

The RF front-end module is the foundation of these systems, and its integration poses a great challenge. Microelectronics technology, since the invention of the transistor, has revolutionized many aspects of electronic products. This integration and cost path has led the microelectronics industry to believe that this kind of progress can go on forever, leading to so-called "system-on-chip" (SOC) for all applications. But it is becoming clear that the production of a complete solution for the new wireless communication front-end is still a dream. When you consider the characteristics of an RF front-end module

- high performance up to 100-GHz operating frequency
- a large number of high-performance discrete passive components
- design flexibility
- reconfigurable architecture
- low power consumption
- compactness
- product customization
- short time to market and low cost

the system-on-package approach (SOP) has emerged as the most effective to provide a realistic integration solution because it is based on multilayer technology using low-cost and high-performance materials [1], [2]. Multilayer topology high-density hybrid interconnect schemes, as well as various compact passive structures, including inductors, capacitors, and filters, can be directly integrated into the substrate. Thus, a high-performance module can be implemented while simultaneously achieving cost and size reduction.

This article illustrates the performance of the next-generation SOP integrated module, including

- the features of the SOP concept for RF front-end module integration
- development efforts on the embedded passive library and 3D modules for wireless applications
- high-performance, organic-based, multichip-module (MCM) technology.

What Is RF-SOP?

In the future, wireless communication will require better performance, lower cost, and smaller RF front-end size. To meet critical specifications, it is common to use discrete passive components, such as surface acoustic wave (SAW) filters and packaged inductors. Although much effort has been devoted to the realization of SOC in RF areas using Si based technology, SOC is considered a solution for limited applications, such as Bluetooth. The recent development of materials and processes in packaging makes it possible to bring the concept of SOP into the RF world to meet the stringent needs of wireless communication. RF-SOP is "to provide a complete packaging solution for RF module by integrating embedded passives components and MMIC at the package level" [3], [4].

To explain the concept, a general system configuration of a wireless transceiver is shown in Figure 1. The module is composed of a monolithic microwave integrated circuit (MMIC) chipset [power amplifier (PA), low-noise amplifier (LNA), up-and-down mixer (MIX), and voltage-controlled oscillator (VCO)] and passive components (filter, antenna, and external high-Q discrete passive elements for blocks with stringent requirements, such as PA and VCO). The RF-SOP approach includes

- the replacement of the discrete passives with embedded ones
- the addition of more functional blocks, such as an antenna, to the module
- the optimization of the performance of the MMIC chipset by replacing on-chip passives with high-Q passives embedded in the package.

Figure 2 is a roadmap for the RF-SOP approach. It is important to note that choice of the on-chip or off-chip (on-package) passives is dependant on the frequency band, modulation scheme, available device, and packaging technology. For example, the linearity and efficiency of PA will determine the choice of an on-chip / off-chip matching circuit. In VCO, the need of a high-Q inductor on package is de-

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termined by the phase noise specification that is coming from a modulation scheme

The advantages of RF-SOP are

- lower cost by using embedded passive instead of discrete components
- design flexibility for MMIC designers by using high-Q passives embedded in the package
- minimized loss and parasitic effects by reducing the number of interconnections
- reduced module size by adopting multilayer packaging
- ease of realization of multifunctional RF modules in a single package
- better high-power handling capability than MMIC chip.

However, there are still some of problems to be overcome, such as

- interference between each of the blocks in a package
- too many degrees of freedom in multilayer packaging to build a design library
- size constraints, if an antenna is included in the package.

Embedded Passive Developments

Mulitlayer Inductor Library

An inductor library for the low-temperature co-fired ceramic (LTCC) packaging process was built based on the multilevel signal line and ground plane concept in Figure 3 [5]. Figure 4 shows three different inductor topologies in microstrip configuration that can be implemented in multilayer board technology. The conventional planar spiral inductor is fabricated on a single layer. Increasing inductance is obtained by increasing the number of turns laterally. As the area increases proportionally to the number of turns, R_S, C_S, and L_S increase while R_P decreases. Therefore, this topology is expected to have both low Q and self-resonance frequency (SRF). The "offset" 3D style, shown in Figure 4(b), offsets the bottom turn so that the upper and lower turns do not overlap each other. While this design has a better SRF due to a slight reduction of C_C, by avoiding the winding overlap, it requires a longer line and, therefore, larger area to get an equivalent inductance to that obtained by the conventional 3D inductor. Figure 4(c) shows a helical configuration which is an evolution of the conventional 3D structure where only half of the turn is fabricated on each layer thereby increasing the gap between two overlapping layers. This architecture occupies the same real estate as conventional 3D structures with reduced C_C due to increasing the gap between the inductor windings and, therefore, improves the SRF.

An 8.2-nH inductor with 10-mil line width using the planar spiral, offset 3D, and helical configurations has been designed, fabricated, and measured. The performance of these three inductors was assessed in terms of Q, SRF, and area. Figure 5 shows that all inductors have a nominal effective inductance of approximately 8.2 nH. We demonstrated that the novel helical type has a three times better Q and twice higher SRF than the planar spiral design while occupying significantly less lateral area compared to the other two types (Figure 6). The performance summary of the three 8.2-nH inductors (Table 1) indicates that the novel helical inductor is not only superior in terms of Q and SRF, but also occupies area an order of magnitude smaller than that occupied by the planar spiral inductor.

Mulitlayer Capacitors

Conventional metal-insulator-metal (MIM) capacitors in microstrip configuration are incorporated for the capacitor library [6]. A capacitance of 0.48fF / mil^2 can be achieved using standard 3.6-mil-thick tapes. A 4.9-pF MIM, for example, can be realized by 100×100 mil square electrodes neglecting the fringing fields. For large capacitors such as the RF ground capacitors, however, the electrode size becomes impractical.

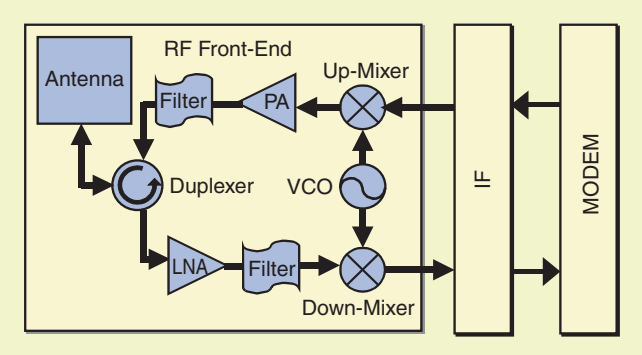


Figure 1. *RF transceiver architecture.*

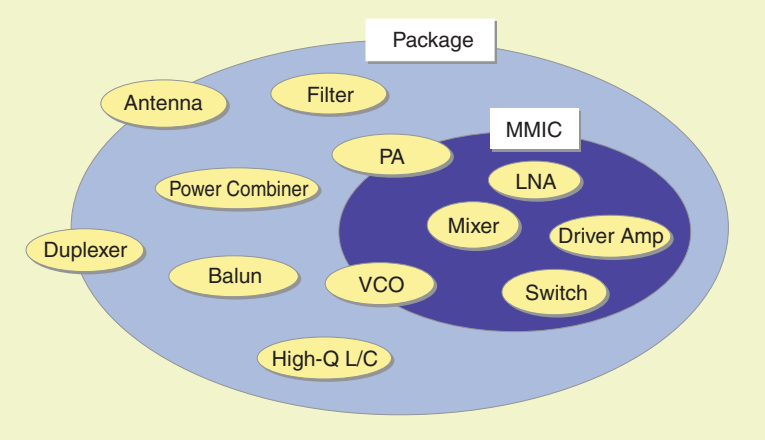


Figure 2. *RF-SOP road map.*

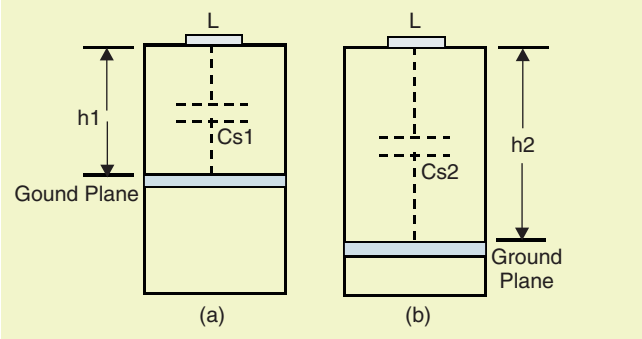


Figure 3. *An illustration of multilevel signal lines and ground plane inductors.*

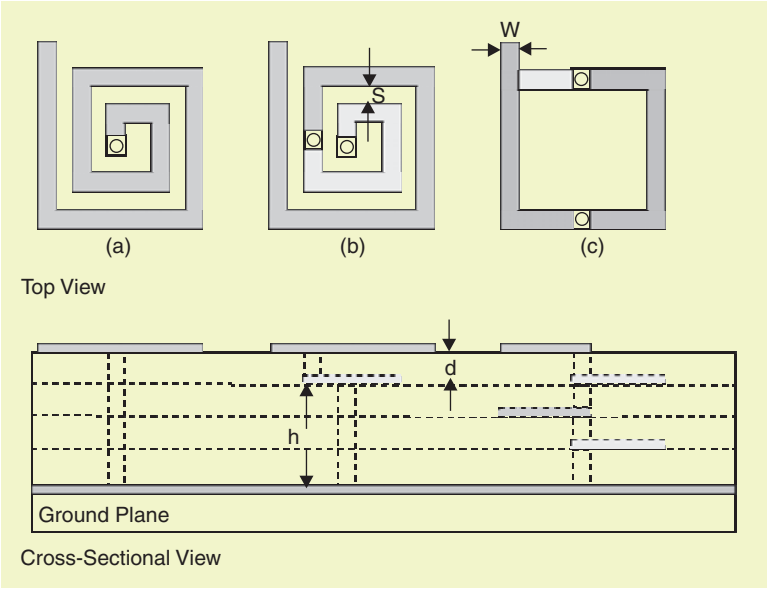


Figure 4. *(a) Top and cross-sectional view of a planar spiral, (b) offset 3D, and (c) helical inductors.*

Therefore, there is a need for a new configuration to maintain the compactness of the capacitor structures. The lateral electrode interdigitation method has been applied to implement a capacitor as well. While exhibiting less parasitics, this topology tends to require a bigger area, considering that the electric flux is generated laterally instead of vertically, such as in the MIM case, which allows more electrode coverage and, thus, occupies less area.

An alternative capacitor implementation to the MIM topology was proposed using the vertically interdigitated configuration (VIC). Figure 7(b) illustrates the concept of the VIC as compared to the conventional MIM structure shown in Figure 7(a). The MIM structure, consisting of a dielectric layer sandwiched between two square plates of width s in Figure 7(a), neglecting the higher order excitation mode. This capacitor can also be implemented by a parallel combination of pairs of plates of smaller size. The VIC deploys these smaller plates with width s' vertically. The plate size can be made smaller as more plates are deployed on a larger number of dielectric layers. The electric flux not only flows vertically between the pair of the capacitor electrodes, but also laterally between the via interconnects to the electrode. Such a mechanism allows further shrinkage of the VIC plates. VIC topology occupies nearly an order of magnitude less area than the MIM, while maintaining comparable performance.

Mulitlayer Filter

An on-package integrated multilayer filter offers a more attractive implementation than on-chip and discrete filters. An RF image-reject filter was implemented with six layers of LTCC in a stripline configuration, whose 3D view is illustrated in Figure 8. Layers 6 and 0 are the top and bottom metalizations which serve as the top and bottom ground planes. The two shunt inductors, L_1 and L_2, were realized by the U-shaped strips fabricated on layers 4 and 3, which are located two and three layers underneath the top ground plane, respectively. The end of the strips are connected to both grounds through vias. There is no metalization between layer 4 and 6, therefore, the top inductor strip on layer 4 is 7.2 mil (two layers) away from the top ground plane, while the bottom strip is 10.8 mil (three layers) away from the bottom ground plane. The required mutual inductive coupling is achieved by overlapping the L_1 and L_2 strips, which are one layer (3.6 mil) apart. MIM capacitors with electrodes on layers 4 and 3, laid out beside the inductor strips, were utilized to implement C_I and C_O. The VIC topology was utilized to implement C_S, which is realized by two series capacitors of capacitance 2 C_S. Each of

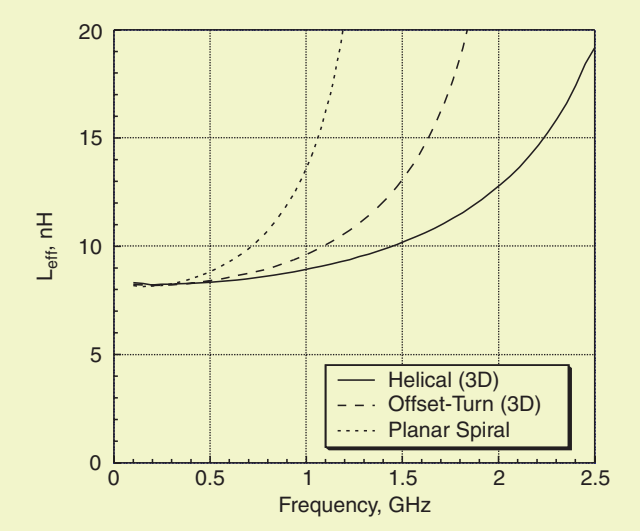


Figure 5. *Measured effective inductance of the planar and 3D inductors.*

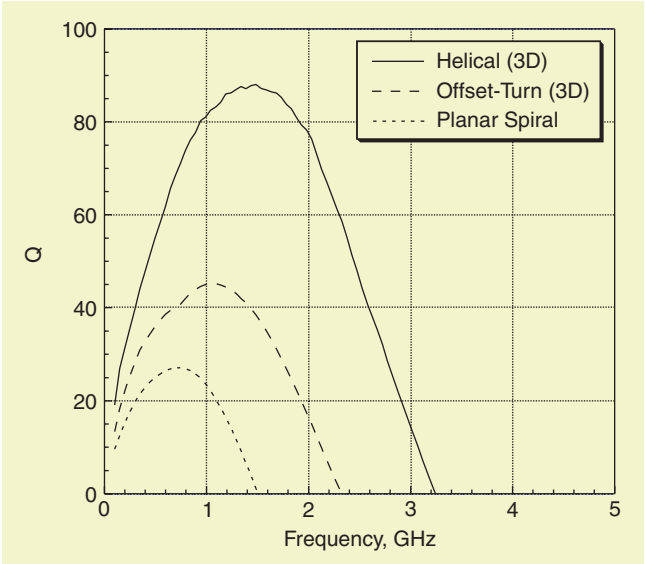


Figure 6. *Measured Q of the planar and 3D inductors.*

these capacitors is implemented in VIC topology as a parallel combination of two capacitors with a value of C_s. Such implementation ensures the symmetry of the structure desirable for high frequency circuits. If C_s were implemented in MIM topology, the entire structure would not have been symmetrical. The bottom plates of C_I and C_O are used as the top plates of the VIC extended to layer 2 through via connections. The dumbbell-shaped trace is inserted on layer 2 between layer 3 and 1 as the bottom plates of the VIC. The extended top plates of the VIC on layer 1 are used as the top MIM electrodes for the shunt capacitor C_R with the bottom ground on layer 0 as the bottom electrode. The filter prototype is given in the photograph in Figure 9. Figure 10 gives the measured insertion loss of 3 dB at 2.4 GHz with 40-dB rejection at 2 GHz.

Table 1. Summary of the three different types of multilayer inductors.

Types	# of turns	D (mil)	Q max	SRF (GHz)	Leff (nH)	Area (mil × mil)
a) Planar spiral	3	-	27 at 0.8 GHz	1.5	8.2	90 × 107
b) Modified 3D	2	7.2	46 at 1.1 GHz	2.3	8.2	74 × 75
c) Helical	2	3.6	88 at 1.3 GHz	3.2	8.2	42 × 37

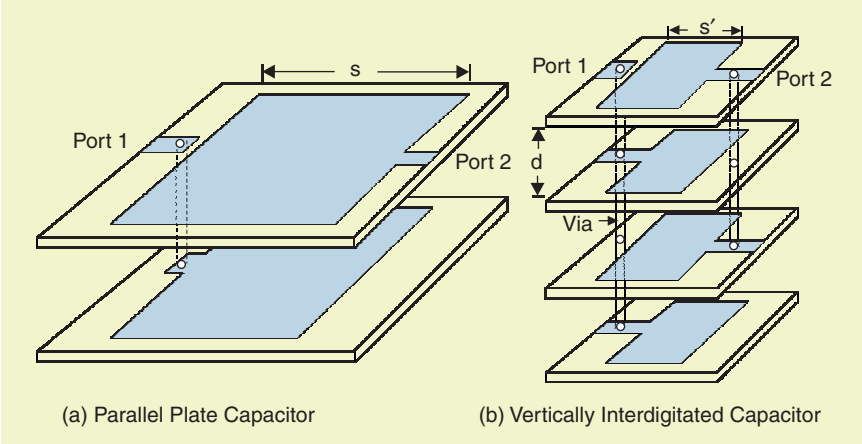


Figure 7. *Three-dimensional views of MIM and VIC configurations.*

Integrated Antenna

One of the major issues in developing RF-SOP is integrating an antenna with a module efficiently. Fabricating an antenna directly on the package has the advantage of reducing feeder loss and size of an entire module. However, for the frequency range from 1-6 GHz, which is being used for most wireless mobile and data communication, it is difficult to bring an antenna into the transceiver module since the size of the antenna becomes large. Also, the interference between the antenna and other RF components in a highly compact module is another main hinderance of this approach.

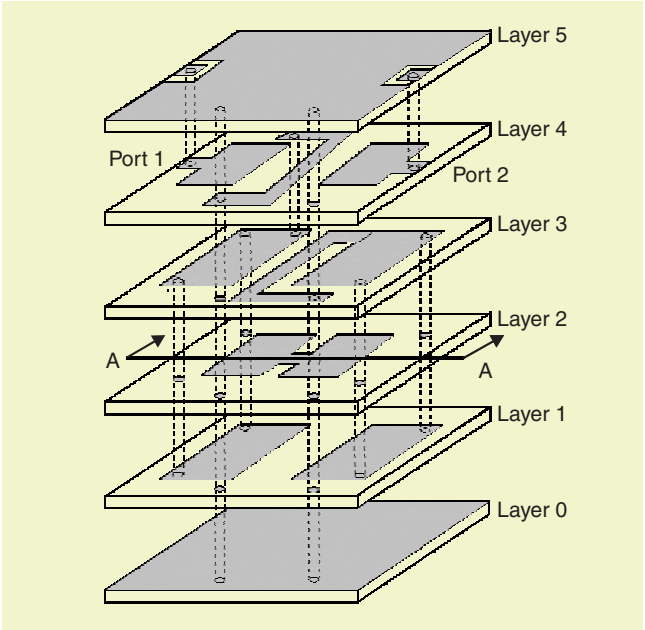


Figure 8. *A 3D layer-by-layer view of multilayer filter structure.*

In compact modules, a cavity-backed patch antenna (CBPA) has been successfully adopted to LTCC packaging (Figure 11) [7]. The antenna is designed to be connected with the embedded RF blocks, such as filter or duplexer switches. The cavity structure is formed by surrounding multiple vias connected to the ground plane. The radiator (patch) is made on the top surface and is connected with the embedded filter through a via. The location of the via feed is designed to get impedance matching with an embedded filter. A CBPA needs a smaller ground plane since most of energy is confined between the edge of the patch and via wall. Obviously, thicker substrate increases the bandwidth of the antenna, but the thickness should be determined moderately by considering the entire module structure.

The measured return loss of the CBPA designed for 5.8 GHz is shown in Figure 12. For comparison, a microstrip patch antenna has been developed for the same frequency. The result shows that bandwidth of a CBPA is 20% larger than the patch.

Multilayer Balun

Baluns are required in a wide variety of microwave components, such as balanced mixers, push-pull amplifiers, multipliers, and phase shifters. They have become important RF components for improving performance and reducing the cost of the RF module by being embedded inside the package.

Figure 13 shows the stripline type multilayer Balun designed for LTCC. Two shorted lines are placed next to an open line such that they couple energy from the open line as shown. Layers 0 and 4 represent the ground planes of the structure.

The half wavelength open line is on layer 2. A small portion of this line is on layer 3 to avoid overlapping traces and to achieve the spiral space saving configuration described previously. One of the quarter wavelength coupling sections is on layer 1 and the other on layer 3. Each of these lines is shorted to the ground planes (through vias) above and below it, respectively.

There is very good agreement between the measurement and simulation, as can be seen from the results (Figure 14). An insertion loss of 3.4 dB was measured, while a measured bandwidth of 41% was calculated compared with 69% for the simulation.

Integrated RF-SOP Modules

Ku-Band Transmitter Module

The implementation of a compact transmitter module is the key issue for higher data rates and broadband transmission, such as applications of satellite communication systems in the Ku/Ka-band range. One obstacle for a compact transceiver module is the large and heavy cavity filter that cannot be easily integrated into the module.

A highly integrated LTCC based transmitter module using GaAs metal-semiconductor field-effect transistor (MESFET) MMICs for Ku-band satellite communication applications is presented [8]. Figure 15 shows the 3D-configuration and picture of the module. The upconverter MMIC integrated with a VCO exhibits a measured upconversion gain of 15 dB and an IIP3 of 15 dBm, while the power amplifier (PA) MMIC shows a measured gain of 31 dB and a 1-dB compression output power of 26 dBm at 14 GHz. Both MMICs were integrated on a compact LTCC module where an integrated front-end band pass filter (BPF) with a measured insertion loss of 1.8 dB at 14.5 GHz was integrated. The bandpass filter for the transmitter module was implemented in a coupled line filter topology on a multilayer LTCC substrate. The two stripline ground planes are physically connected by vias, and the actual input and output of the filter are connected to the RF amplifier and driver amplifier of the transmitter. Three segment folded edge coupled strip-line filters, where the middle segment was deployed perpendicular to the first and third segments for compactness, have been designed to suppress the local oscillator (LO) signal at 13 GHz as well as the harmonics and spurious signals. This is a balanced stripline topology where the coupled-line segments are sandwiched by two ground planes at an equal distance of 17.6 mil (four LTCC tape layers).

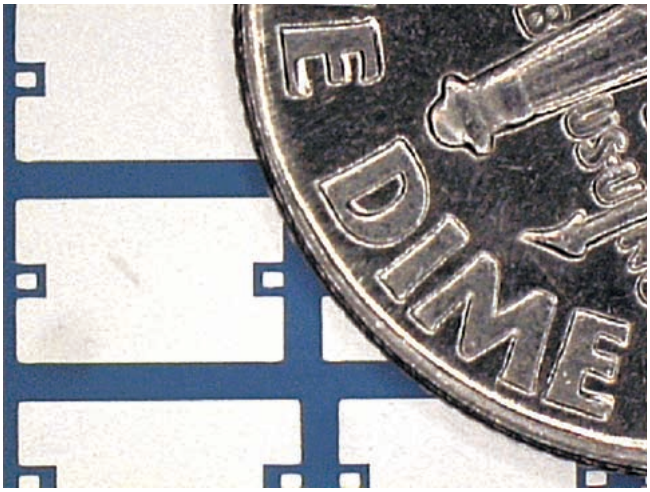


Figure 9. *Photograph of the fabricated filter.*

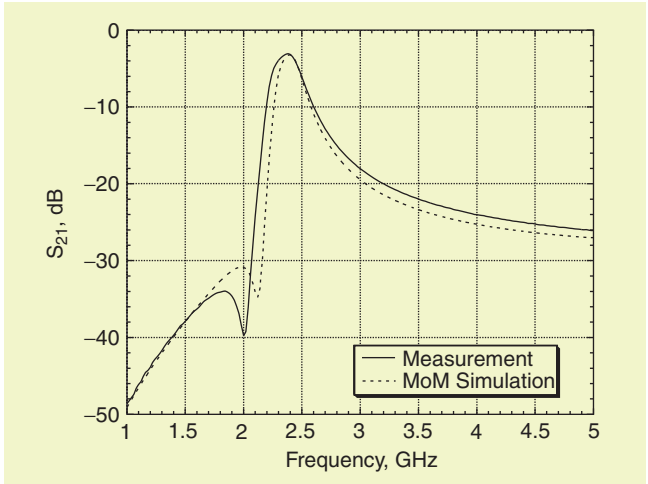


Figure 10. *Measured and simulated magnitude of S_{11} and S_{21} for the filter.*

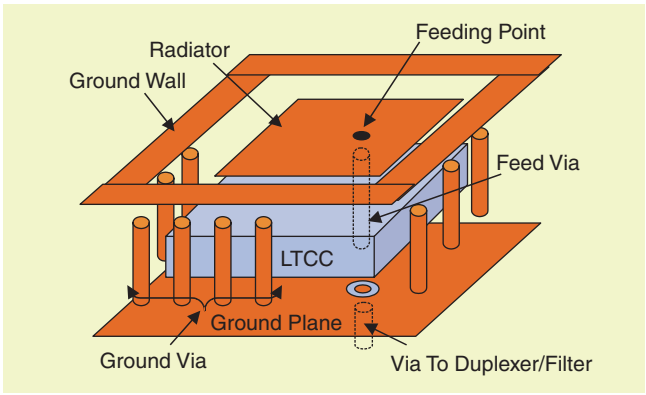


Figure 11. *Configuration of CBPA.*

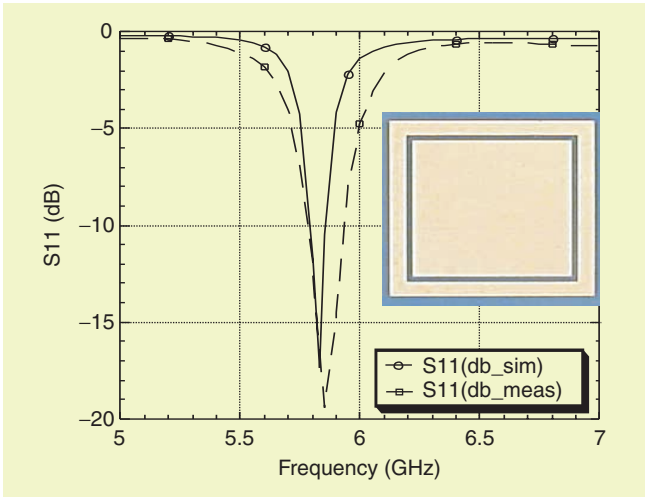


Figure 12. *Measured and simulated return loss of the CBPA designed for 5.8 GHz.*

The entire transmitter chain exhibits a total gain of 41 dB and output power of 26 dBm incorporating the wirebond loss from 14-15 GHz and image rejection of more than 30 dBc at 12 GHz [Figure 16(a)]. Figure 16(b) shows the overall system level diagram of the entire transmitter chain based on the measurement of each transmitter block. The compact module was made possible by embedding the filter, thereby saving more than 40% of real estate compared to the module if it were implemented on a typical alumina substrate.

3D-Integrated Module for C-Band

The integration of the antenna and the RF front end in a compact module is quite attractive and challenging. Several works on modules in which the antenna has been integrated have been presented for mm-wave wireless applications [9]. These techniques are difficult to adopt in C-band due to the larger relative size of the antenna at the frequency of interest. A 3D integrated transceiver module with an antenna for 5.8 GHz is presented here [10]. The structure of the integrated module is shown in Figure 17. Three different layers for the transceiver, filter, and antenna, are vertically stacked and connected through vertical vias. The antenna and filter are directly fabricated on the module using LTCC technology in order to reduce size and interconnection losses.

The module has been designed for 20 LTCC layers. Before designing each of the embedded passives, the layers are properly assigned. The antenna, filter, and transceiver utilize 8, 10, and 2 layers, respectively. The total size of the module is $14 \times 19 \times 2$ mm^3, including all the RF functional blocks. The grounds are connected efficiently to suppress the unwanted parasitic modes. A photograph of the integrated module is shown in Figure 18.

To utilize the module space effectively, the type of passive components should be chosen very carefully. A CBPA has been designed for the module. A three-section coupled stripline filter has been designed to be embedded inside of the LTCC package. The input and output ports of the filter are connected to the antenna and the duplexer switch through vias. RF functional blocks, including PA, LNA, mixers, and VCO, are attached on the top of the LTCC board. The specifications of the functional blocks have been determined and verified through system simulations based on IEEE 802.11a. To evaluate the performance of the module, each of the sections in the module have been fabricated. The results of this evaluation are shown in Figure 19.

Integrated Power Amplifier Module

A two-stage 1.9-GHz power amplifier with second-harmonic tuning circuits using silicon N-MOSFETs has been built utilizing the LTCC package [11]. Figure 20 shows the schematic diagram and photograph of the LTCC power amplifier. A single-ended two-stage common source amplifier is implemented with an integrated reactive matching network using

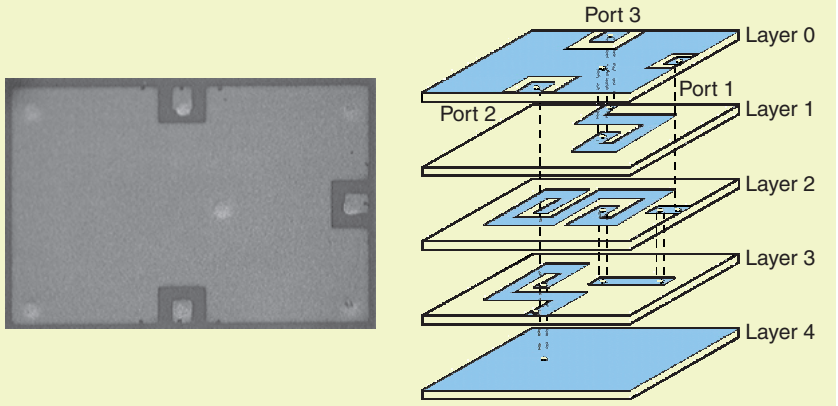


Figure 13. *Photo and configuration of the stripline multilayer balun.*

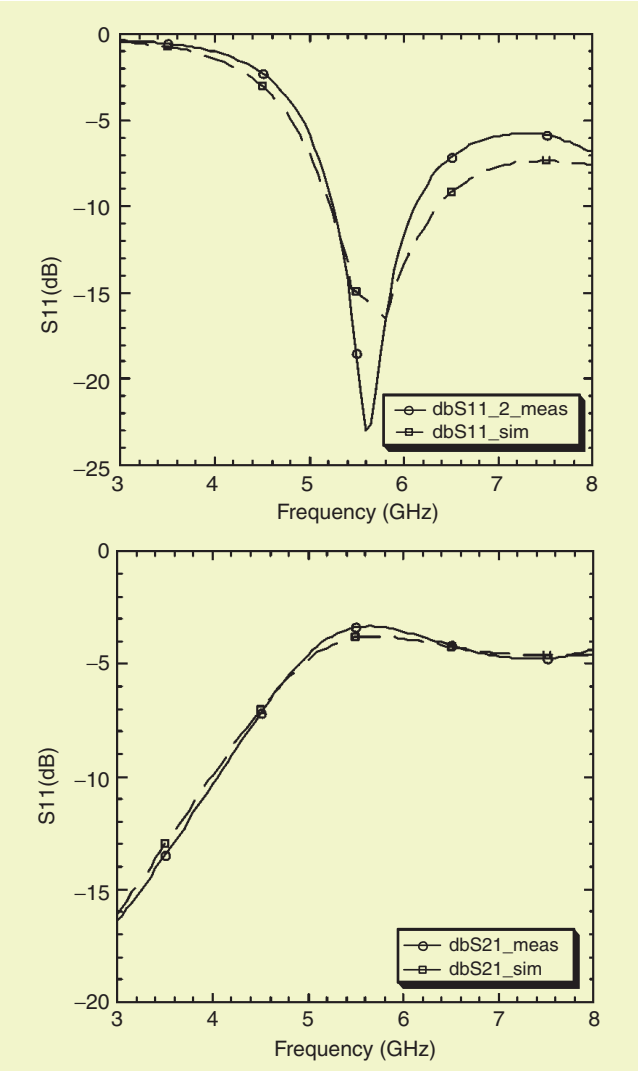


Figure 14. *Measured and simulated results of the stripline balun desgined for 5.8 GHz.*

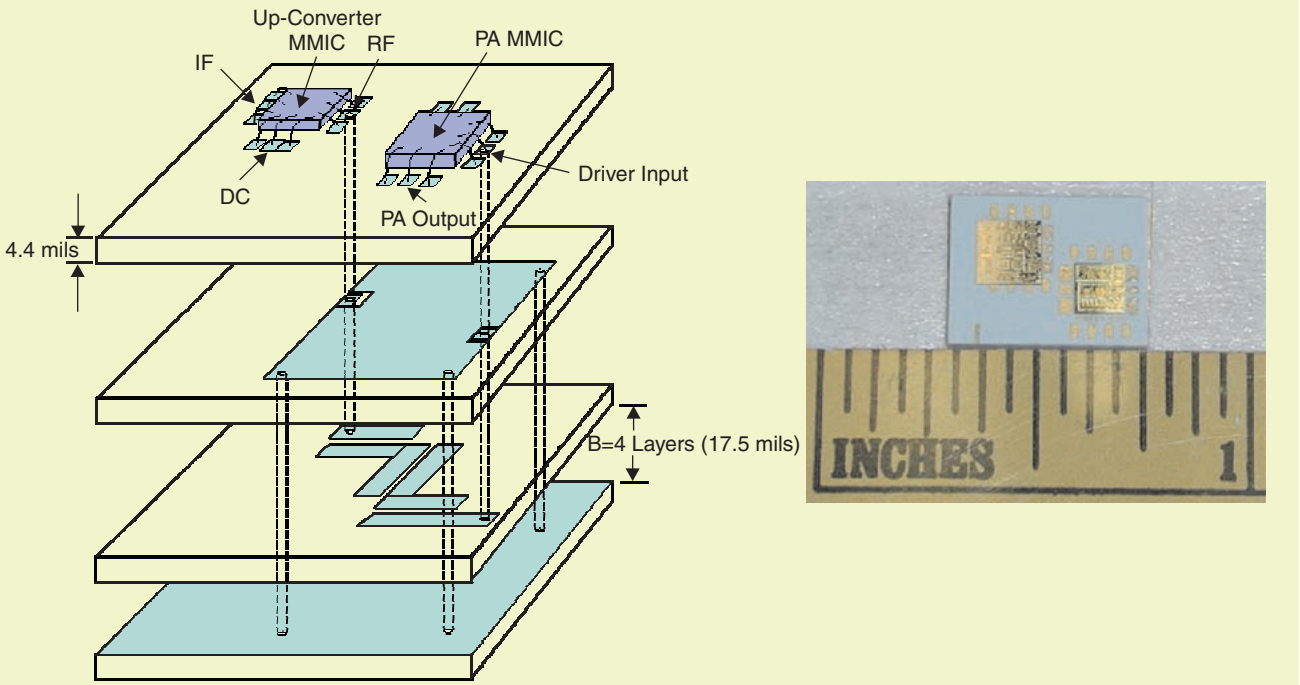
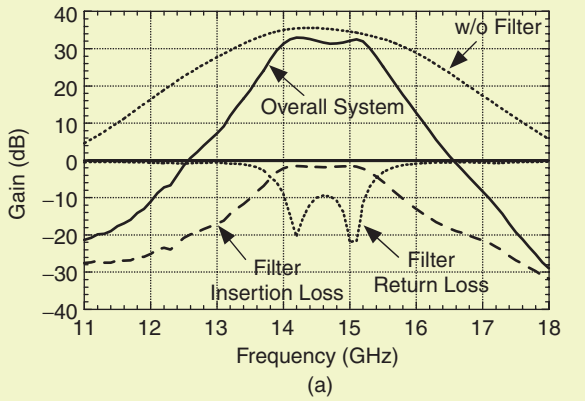


Figure 15. *Configuration and picture of compact Ku-band transceiver module.*



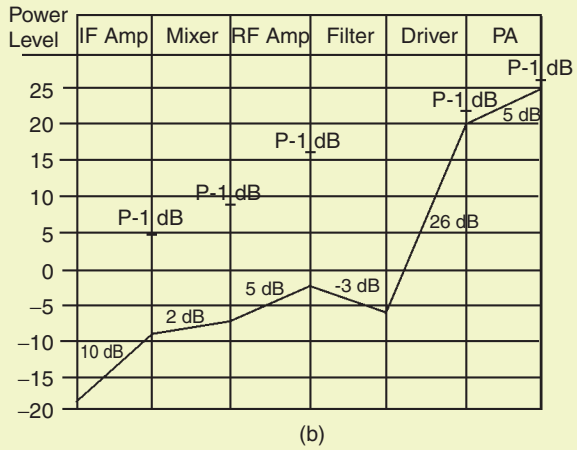


Figure 16. *Measured gain of the module (a) overall system gain and (b) gain variation at each level.*

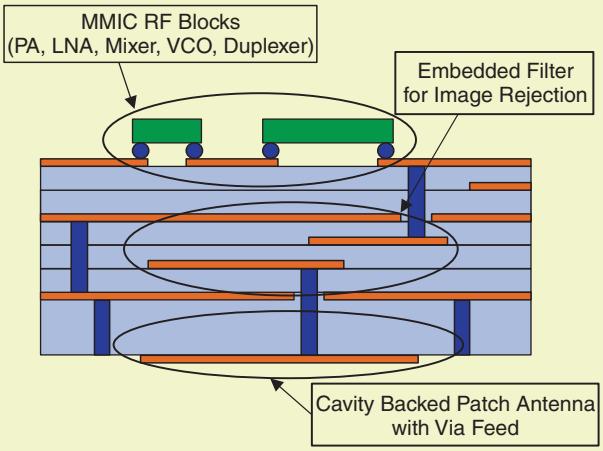


Figure 17. *3D integrated module with CBPA and embedded filter.*

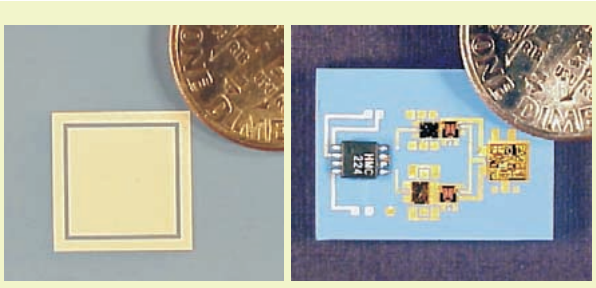


Figure 18. *Photograph of the integrated module.*

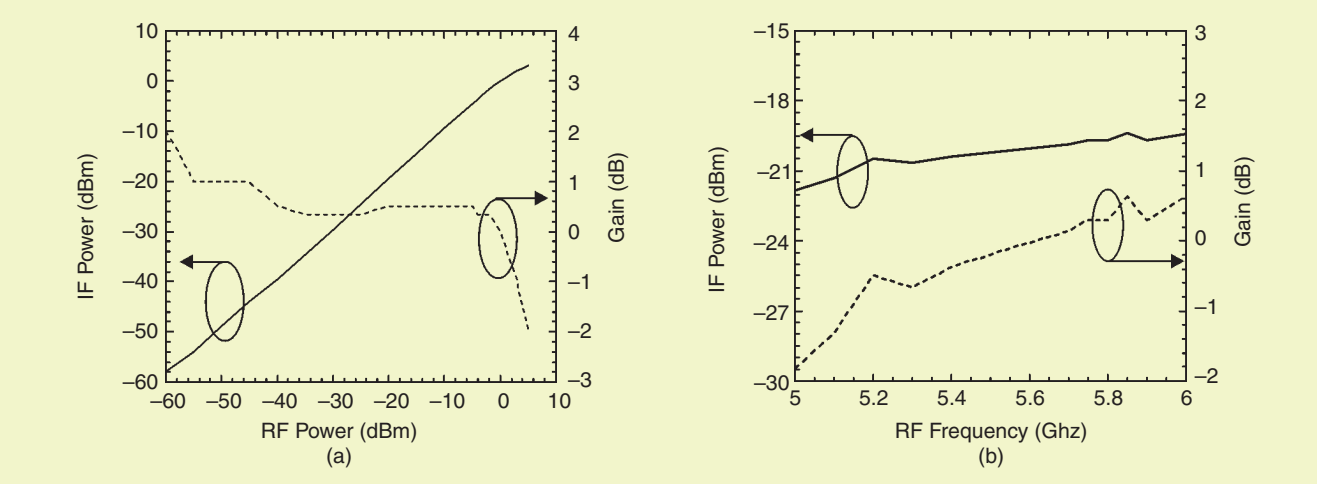


Figure 19. *Measured gain of the receiver versus (a) input level and (b) frequency.*

multilayer LTCC passives. For high-efficiency operation, each stage of the PA was class AB biased (20% of I_{max}), incorporating second-harmonic tuning circuits in the input and output of each stage. The two N-MOSFET devices fabricated in a conventional 0.8-µm BiCMOS technology were wirebonded onto gold pads on the LTCC board. Half- and quarter-turn inductors were used as matching components while a full-turn inductor was used for an RF choke. Parallel- plate MIM capacitors were utilized as matching components for the fundamental signal since their values and sizes are relatively small. The RF ground capacitors were implemented in the compact VIC topology since they require large capacitance value for 1.9-GHz applications. Second-harmonic tuning elements were implemented through a series inductive- capacitance (*LC*) resonator at 3.8 GHz as part of the second-harmonic trap network to improve the efficiency.

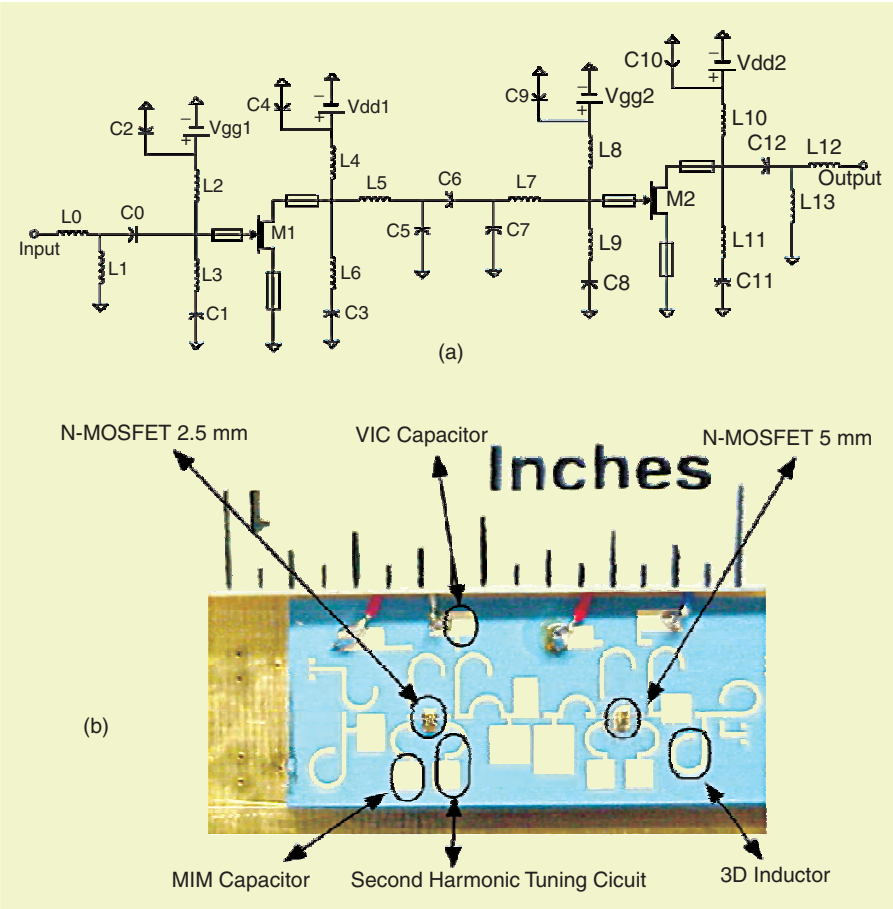


Figure 20. *Schematic diagram (a) and die photo (b) of the 1.9-GHz power amplifier module with fully on-package passives.*

Figure 21 shows the measured gain, power-added efficiency (PAE) and output power of the fabricated CMOS-LTCC PA at 1.9 GHz. The power amplifier exhibits 48% PAE, 26-dBm output power, and 17-dB power gain at 1.9 GHz with a 3.3-V drain supply voltage.

To investigate the advantage of integrating passives on-package, such as on LTCC, another 1.9-GHz power amplifier was built with the same topology as that with fully integrated LTCC passives. The two-stage CMOS power amplifier integrated the interstage matching components on-chip, while the input and output matching elements, as well as the RF choke and ground inductors and capacitors, were integrated on LTCC using the library components. Figure 22 shows the circuit schematic and a photograph of the LTCC board housing the module. The fully monolithic on-chip version of this power amplifier using the same CMOS technology and the same schematic has also been designed, fabricated, and measured. Table 2 outlines the measured performance comparison of the 1.9-GHz power amplifier, employing three different passive integration ap-

proaches: fully LTCC integrated, on-chip interstage integrated, and fully on-chip integrated techniques. These results clearly demonstrate the advantages of implementing on-package components where superior Q performance can be achieved.

Multilayer Organic Package

A multilayer packaging process using a organic material, developed by the Georgia Institute of Technology's Packaging Research Center, offers potential as the next generation technology of choice for SOP for RF-wireless, high-speed digital, and RF-optical applications [12]. This approach set up the technological platform with the ability to integrate on the same substrate digital, RF, and optical systems.

The current SOP configuration is shown in Figure 23. It incorporates low-cost materials and processes consisting of a core substrate (FR-4 for example) laminated with two thin organic layers. The thickness of the core substrate is 40 mil, while the thickness of the laminate layers are 2.46 mil each.

The integral passive components fabricated within the wiring structure of the SOP module, which consists of a three metal layer structure, including two layers of high-density wiring metallization and two micro via levels. For this multilayer interconnection structure, 10-18-µm copper metallization and 100-µm diameter micro vias process are used. The minimum metal line width and spacing is 1 mil for the top two metal layers.

Multilayer Inductors

High Qs at the frequency range of interest can be obtained by designing multilayer inductors and HGP inductors using multilayer organic technology. The CPW spiral inductor (Figure 24) avoids via losses, has reduced dielectric losses, and increased SRF. Also, the thick copper metalization in the packaging process make it possible to get a very high-Q. This decreases the shunt parasitic capacitance and reduces the eddy current flowing in the ground plane, producing negative mutual inductance effect. As a result, higher Q and L_{eff} can be achieved. The CPW inductor demonstrates a Q of 182, an SRF of 20GHz, and a L_{eff} of 1.97 nH, as shown in Figure 23.

Embedded Filters

Several embedded filters were designed for the process. The bandpass filter design for C band applications consists of a square patch resonator with inset feed lines (Figure 25). The inset gaps act as small capacitors and cause the filter to have a pseudo-elliptic response with transmission zeros on either side of the passband. This structure also has a tunable bandwidth. The length of the insets and the distance between them are the main controlling factors, effectively setting the size of the mode-splitting perturbation in the

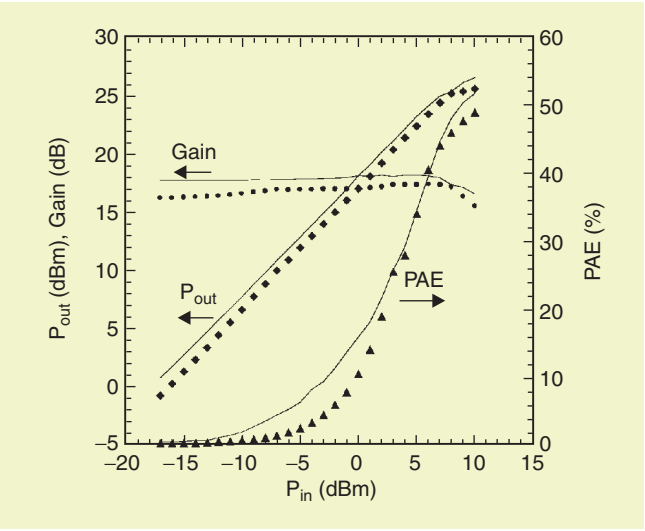


Figure 21. *Measured (dot) and simulated (solid) gain, PAE, and output power of the PA at 1.9 GHz.*

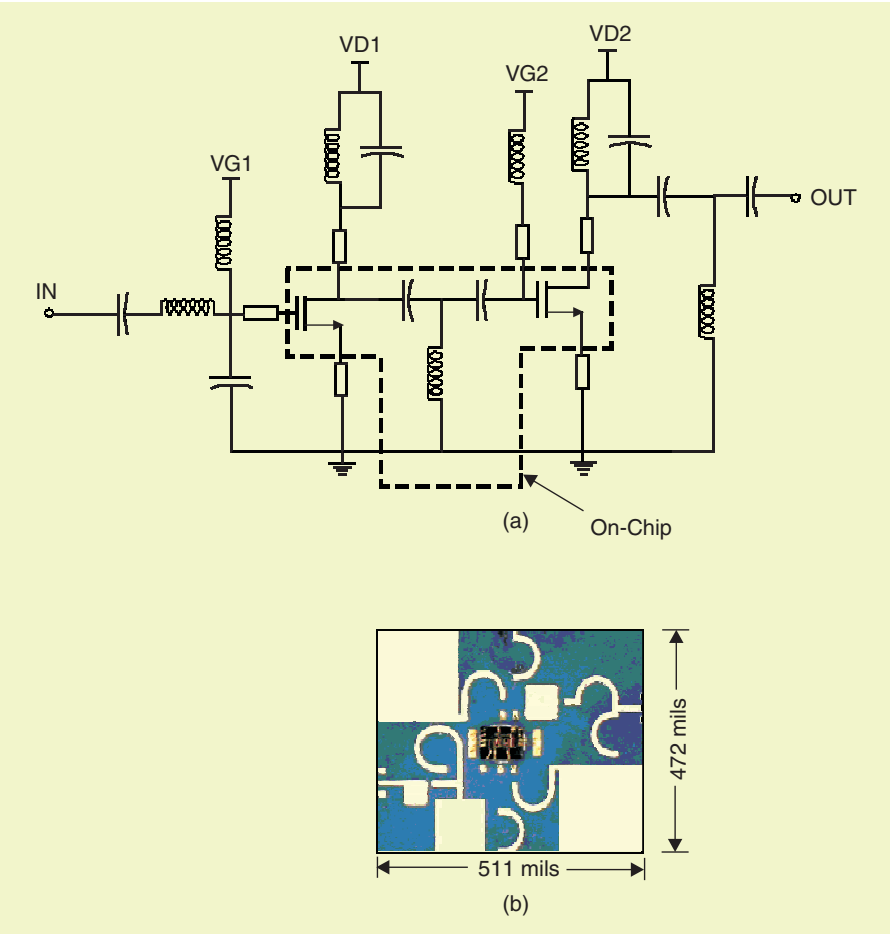


Figure 22. *Schematic diagram (a) and die photo (b) of the 1.9 GHz power amplifier module with on-chip interstage matching and on-package in/output matching.*

Table 2. Comparison of three different approaches of the power amplifier.				
Passive integration	**Pout (dBm)**	**Gain (dB)**	**PAE (%)**	**Area (mil × mil)**
Fully on-package	26	17	48	900 × 500
On-chip interstage	23	15	32	511 × 472
Fully on-chip	19	10	20	105 × 84

field of the resonator. The length of the feed lines is determined by the input and output matching requirements. The measurement results show a bandwidth of 1.5 GHz and a minimum insertion loss of 3 dB at the center frequency of 5.8 GHz.

Other Attributes

In addition to the filter and inductor, many passives are being developed for the organic process. A lifted slot antenna has been successfully implemented in the package. Also, CPW-microstrip transition using vias shows that it can be used up to 20 GHz.

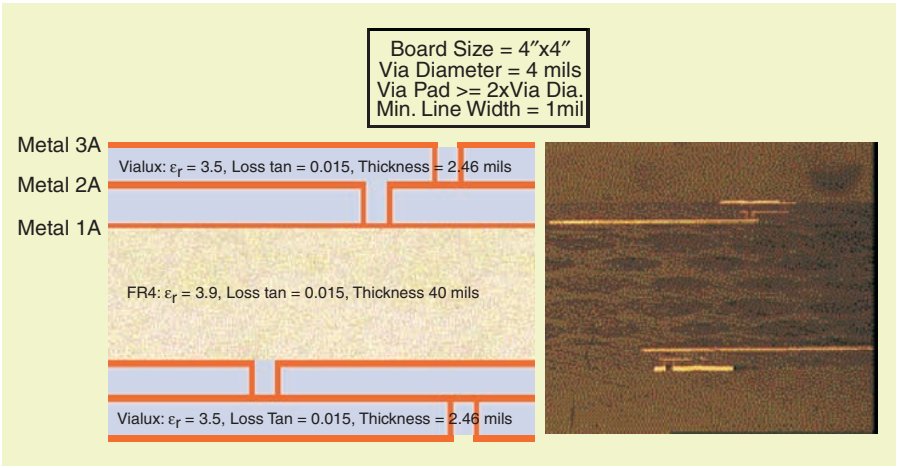


Figure 23. *3D integrated module with CBPA and embedded filter.*

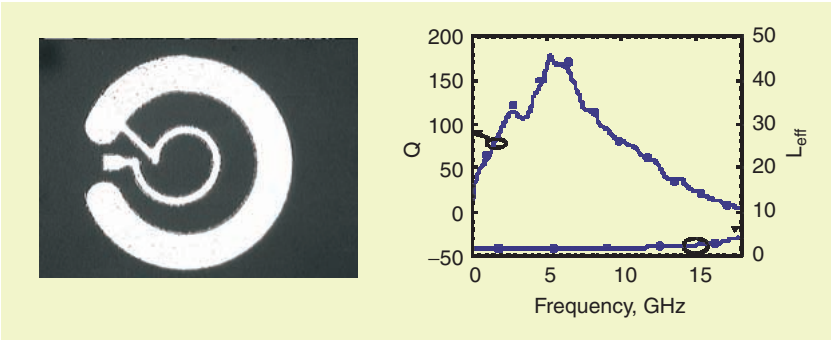


Figure 24. *Photo of CPW inductor and measurement result of Q and inductance.*

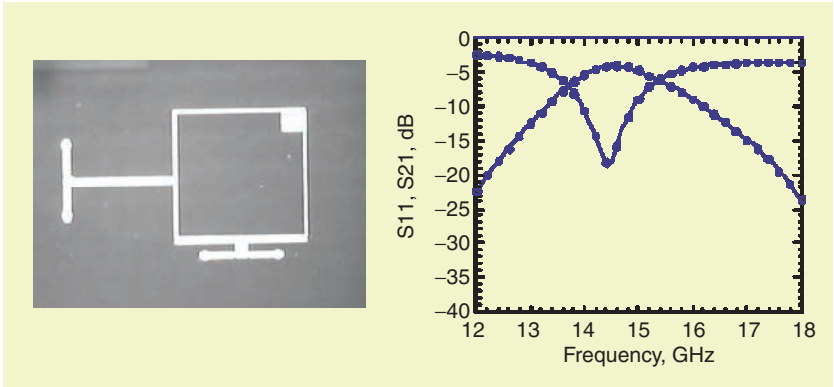


Figure 25. *Photo of bandpass filter for 5.8 GHz and measurement results.*

Conclusion

We have presented the SOP concept applied for RF front-end module integration. The development of an LTCC-based component for wireless RF-SOP applications has been described. Various types of multilayer embedded passive components including inductor, capacitor, filter, antenna, and balun suitable for the highly integrated module have been presented. Development efforts on a 3D integrated module, which includes wireless transceivers and power amplifier modules have been demonstrated, and then a novel 3D integration concept has been described. Multilayer organic packaging developed for SOP was also reported. Very high Q-factor inductors (up to 180) and embedded filters have been presented as examples of the high performances of multilayer organic packages.

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