# Advanced System-on-Package RF Front-ends for Emerging Wireless Communications

## (*Invited paper*)

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***Abstract* – System-on-Package (SOP) is getting more attention in the RF area and is being applied to RF functional blocks and the front-end modules to achieve lower cost, improved performance, and increased design flexibility. In this paper, we present recent developments of RF modules based on the SOP concept. The SOP modules include power amplifier module with embedded harmonic suppression filter, VCO with embedded high-Q inductor, and compact RF-front-ends that were developed by utilizing the ceramic and organic based multi-layer packaging technologies, respectively. The examples in this paper indicate the feasibility of the SOP approach for solving RF issues, which cannot be solved easily with current conventional approaches.**

***Key words:* SOP, WLAN, RF front-end, power amplifier, voltage-controlled oscillator, LTCC, organic package, embedded passives, filter, antenna**

### 1. Introduction

Wireless communications are evolving toward using higher frequencies, wider bandwidth and more functionality to satisfy growing demands of users worldwide. Meeting the stringent system specifications of emerging wireless communication standards and providing support to multi-standards and multi-bands on a single platform, while at the same time trying to keep the cost of the RF-front-end the same or less, is a significant challenge to the RF hardware developers.

In recent years, the concept of System-on-package (SOP) is getting more attention as the RF front-end solution for comprehensive communication systems. SOP can be defined as "a complete single packaging RF module composed of embedded passives and MMICs by utilizing the state-of-the-art multi-layer packaging and the interconnection of technologies."[1] The SOP-based RF front-end will give more flexibility to the RF designers, since it is more cost effective than discrete components based module and more performance effective than the system-on-chip (SOC) solutions.

In this paper, recent developments of RF modules based on the SOP concept and the multi-layer packaging technologies are presented.

Initially, a power amplifier module using a SiGe HBT and the low temperature co-fired ceramic (LTCC) package is presented. At the output stage, the harmonic suppression filter is used to increase the linearity. In addition, the output matching network, has been implemented completely in LTCC without using any external discrete component.

The low cost RF transmitter module developed by the multi-layer organic package (MLO) technology is also presented. The module is composed of the MESFET based up-converter, power amplifier chipset and the band pass filter embedded in the board.

A voltage-controlled oscillator (VCO) module utilizing high-Q inductor is built into the multi-layered organic package (MLO). The phase-noise performance of the SOP-based VCO is better than that of the oscillator using on-chip inductors.

Finally, a 3D-integration RF front-end module for a C-band built by LTCC is introduced. The transmitter and receivers are fabricated on the separate board and stacked using μBGA ball process to reduce the size of the module and minimize the interference between transmitter and receiver. A cavity backed patch antenna and a band selection filter are embedded in the multi-layer substrates.

### 2. Power Amplifier Module with Embedded filter

A 2.4 GHz SiGe HBT power amplifier module with a harmonic suppression filter implemented in LTCC substrate has been developed [2]. The harmonic suppression filter and output match network have been implemented completely in LTCC without the use of external discrete components.

The power amplifier is designed in IBM's commercial SiGe HBT process. It consists of three stages: two driver stages and one power stage; interstage, input and output

match networks, and bias circuits for the three stages. It is packaged in an 8-pin SOIC package. Fig. 1 shows a picture of the developed power amplifier.

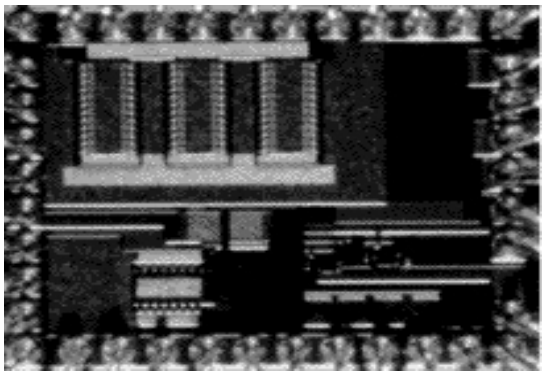


**Figure 1 SiGe power amplifier chip.**

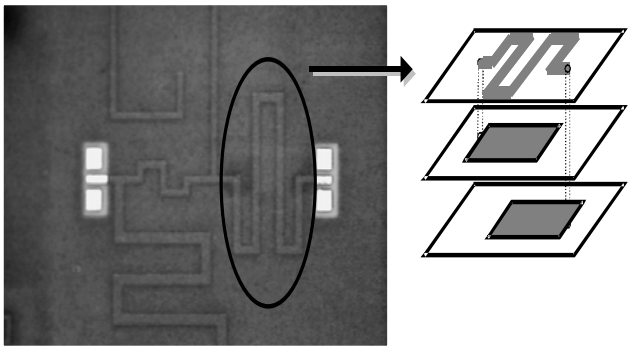


**Figure 2 Output network including harmonic suppression filter and output matching network**

The harmonic suppression filter and output matching networks are designed in Kyocera's 10 layers of LTCC process. Fig. 2 shows the designed filter and output match network. The filter consists of a transmission line in parallel with a capacitor.

The output network is designed to give deep suppression of the second and third harmonics. A $\lambda/4$ length RF-shorted stub is used to achieve a short at the second harmonic. The output matching network, which is also implemented in LTCC using transmission lines, and tuned in conjunction with the harmonic suppression filter presents a short at the second harmonic and nearly an open at the third harmonic.

The output power and efficiency of the power amplifier module is shown in Fig. 3. It achieves an output power of 27 dBm at 0 dBm input with a PAE of 45% at 2.4GHz and Vcc=3.3 V. The linear gain of the power amplifier is 35 dB. The second and third harmonics are – 44 dBc and– 49 dBc, respectively at 0 dBm input.

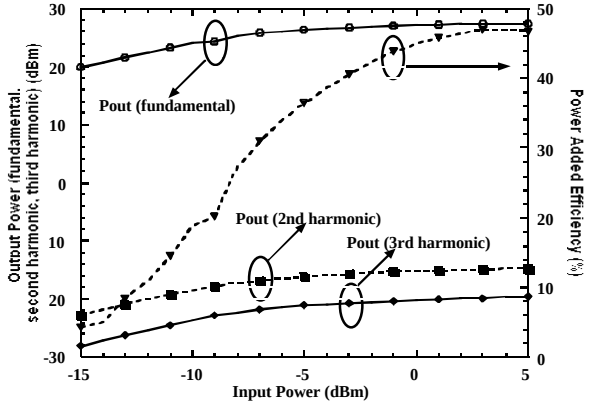
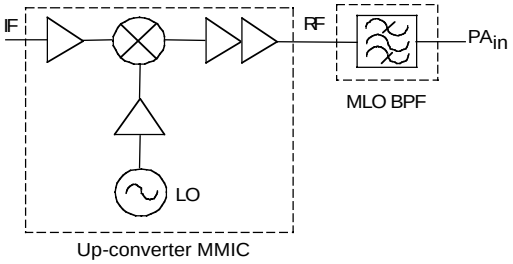



**Figure 3 Measured performance of the power amplifier module**

### 3. RF-front end module using MLO package

Organic material based low cost MCM-L technology is getting more attention even in the RF area due to its low cost feature, and despite such disadvantages as high dielectric loss and too much of process variation. A C-band transmitter module incorporated, an embedded BPF and an up-converter and a PA MMIC is shown in Fig. 4.



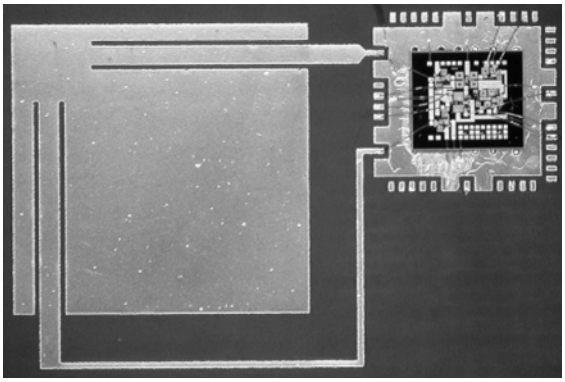



**Figure 4 Schematic and picture of MLO based integrated transmitter module**

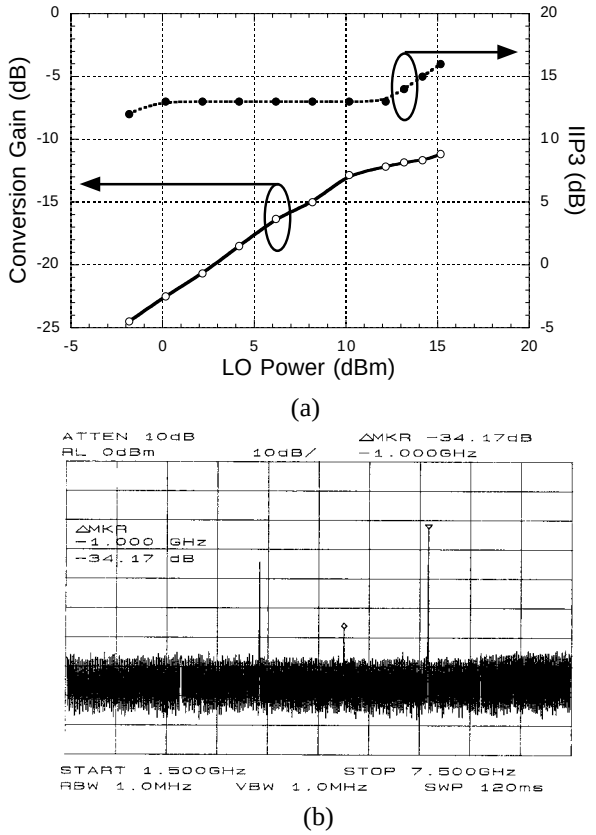



**Figure 5 Measured performance of up-converter chip: (a) Conversion loss, IIP and (b) output spectrum**

The transmitter MMIC provides an excellent LO and image rejection fabricated in a commercial GaAs MESFET process. A miniaturized integrated square patch resonator band pass filter (BPF) with inset feed lines built in MLO technology has been incorporated to realize a compact and highly integrated transmitter module suitable for the low cost network interface card (NIC), IEEE 802.11a WLAN applications in 5-6 GHz frequency band [3].

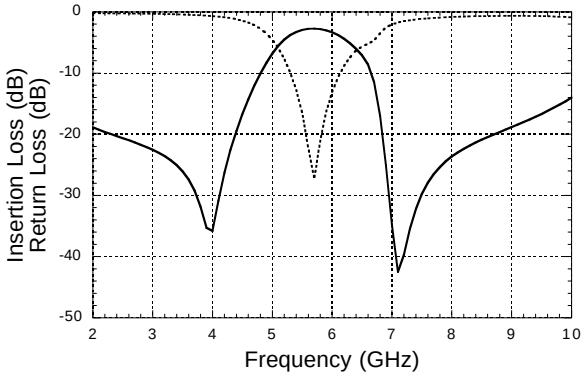



**Figure 6 Measured performance of embedded band pass filter**

The up-converter MMIC consists of a double balanced diode ring mixer (DBM), a wide tuning range (20%) voltage controlled oscillator (VCO), LO buffer amplifier, IF amplifier, and a RF amplifier. The up-converter MMIC integrated with a VCO exhibits a measured up-conversion gain of 14 dB and an IIP3 of 15 dBm as shown in Fig. 5. LO-to-RF isolation is 45dB and image rejection of 11 dBc without any bandpass filtering. MLO-based BPF has been implemented and the measured data is shown in Fig. 6. The BPF shows an insertion loss of less than 3 dB and a return loss of 27 dB at 5.8 GHz as well as the image rejection of 35 dBc at 3.8 GHz.

## 4. VCO with High-Q Embedded Inductor

A C-band oscillator with external high-Q inductors was built in MLO package [4]. All circuit blocks except the inductors are implemented in MESFET MMIC. The inductors embedded in package have been designed to obtain a maximum quality factor around the oscillation frequency.

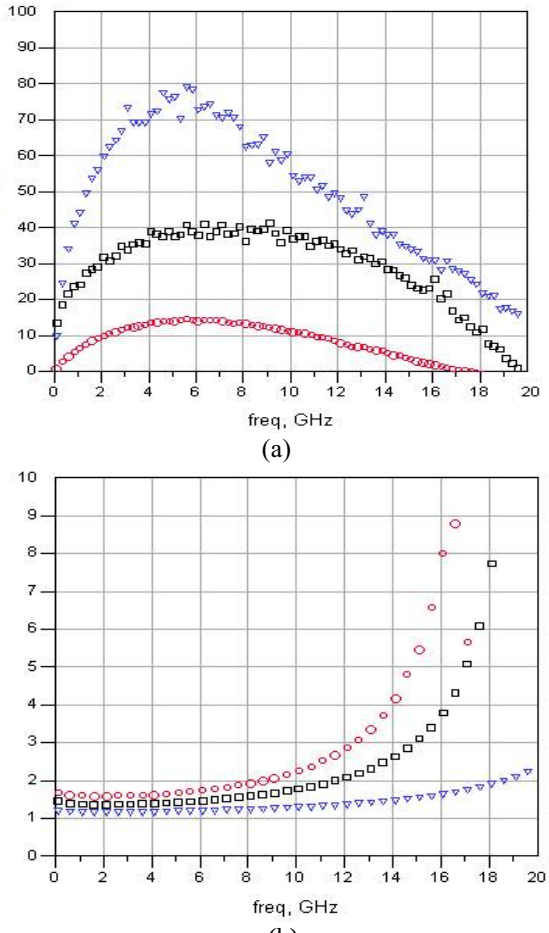
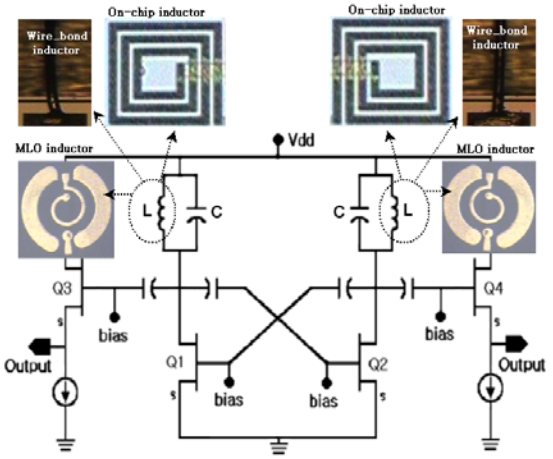


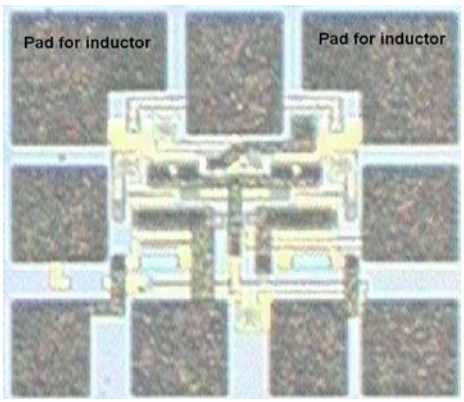

**Figure 7 Comparison of the inductors, On-chip, embedded in MLO and wire-bonding inductors: (a) Q-factors and (b) Inductances**

To validate the VCO with an embedded inductor, the same topology of oscillators having the on-chip inductors, and wire-bonding inductors have also been developed and compared. All the inductors have been designed to get the inductance value of approximately, 1.5nH and optimized

to get the highest quality factor in C-band. The measured performances of the three inductors are shown in Fig. 7.




(a)




(b)

**Figure 8 Developed oscillator: (a) schematic and (b) MMIC chip**

The schematic of the oscillator is depicted in Fig. 8. The TriQuint 0.6 µm GaAs MESFET process is utilized to design and implement the oscillator circuit. To reduce the 1/f noise up-conversion, the cross-coupled differential topology with the capacitive coupling feedback was used. Cross-coupled transistors (Q1 and Q2) form a positive feedback to provide a negative resistance to cancel the loss in the LC-resonators. The positive feedback is obtained through capacitors (Cf) that take the role of suppressing the 1/f noise up-conversion as well as dc blocking in order to bias cross-coupled transistors.

The measurement result of the oscillator with MLO inductor is shown in Fig. 9. On-wafer measurements of the oscillation frequency, output power, and phase-noise were performed using an Agilent 8563E spectrum analyzer. The phase-noises of the oscillator with the embedded inductor and the on-chip inductors are –108 dBc/Hz and –113 dBc/Hz at 600 KHz offset frequency, respectively. Using MLO inductors, the phase-noise is better than the oscillator with on-chip inductors and comparable to the oscillator with wire-bond inductors.

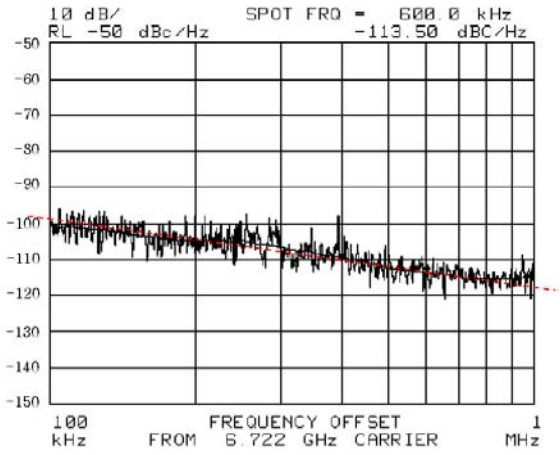



**Figure 9 Phase noise measurement result for the oscillator with MLO inductor**

## 5. 3-D RF Module Development

We also present a very compact 3D-integration concept suitable for a RF front-end module by means of substrate stacking method using µBGA ball process [5]. (Fig. 10 illustrates the proposed module concept)

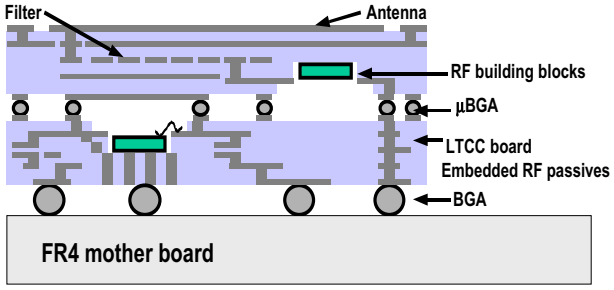
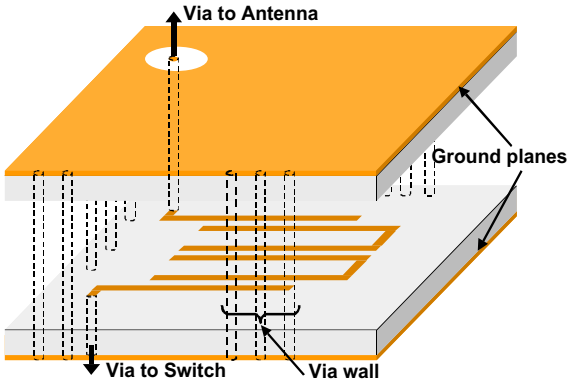


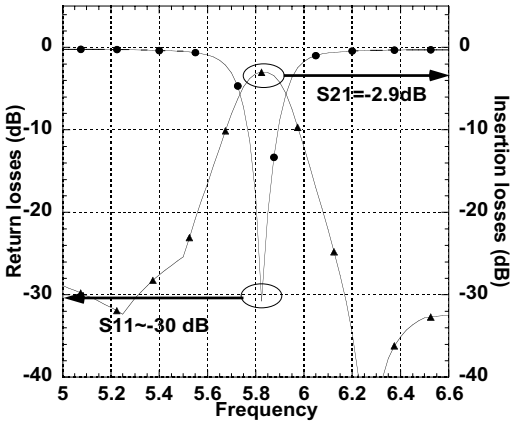

**Figure 10 Proposed 3D Integrated RF front-end concept**

Two stacked LTCC substrates are used and board-to-board vertical transition is realized by µBGA balls. The top and the bottom substrates are dedicated respectively to the receiver and transmitter building blocks of the RF front-end module. Tests structures have been designed for the characterization of µBGA balls and an accurate µBGA ball modeling shows insertion loss less than 0.1 dB and return loss of - 17dB up to 10 GHz.

We have developed a high performance second order narrow-band band-pass filter with two cascaded coupled line sections embedded in strip-line configuration to improve insertion loss. A schematic view and measured performance are presented in Fig. 11. Coupled lines have been bent to fit into the module shape and via walls are used to connect ground planes and reduce parallel plate modes. Filter performances have been measured separately and exhibit a –2.9dB insertion loss, – 20.8dB return loss, and image rejection greater than –20 dB as shown in Fig. 12.




(a)

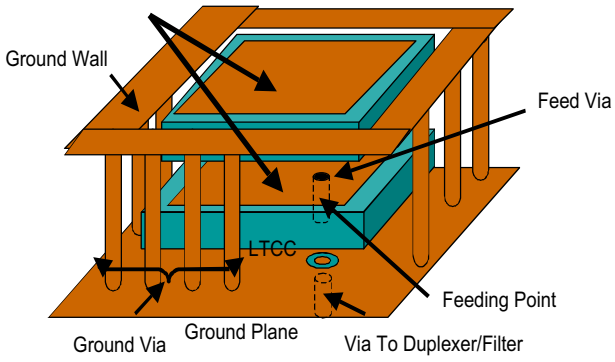



(b)

**Figure 11 Embedded filter; (a)schematic and (b)performance**

A via-fed stacked cavity-backed patch antenna has been designed for IEEE 802.11a 5.8 GHz band as shown in Fig. 12 [6]. The heights of the lower and upper patches (400 mils × 400 mils) are 8 mils and 32 mils, respectively. The 10-dB return-loss bandwidth of the antenna is about 4%, fully covering the required band (5.725-5.825 GHz).

The commercial 0.6um GaAs MESFET process was used to implement Rx and Tx chipset. Photo of upconverter chip is shown in Fig. 13.



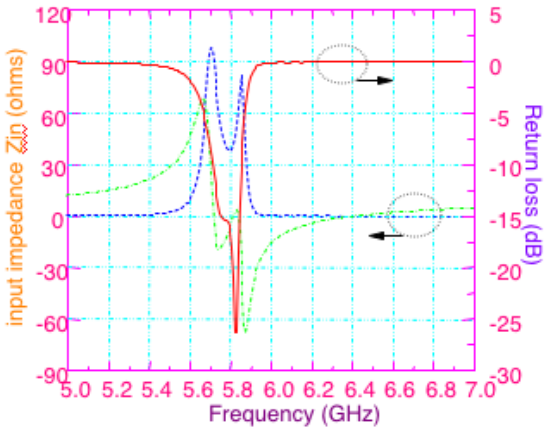




**Figure 12 Cavity backed patch antenna layout and performance**

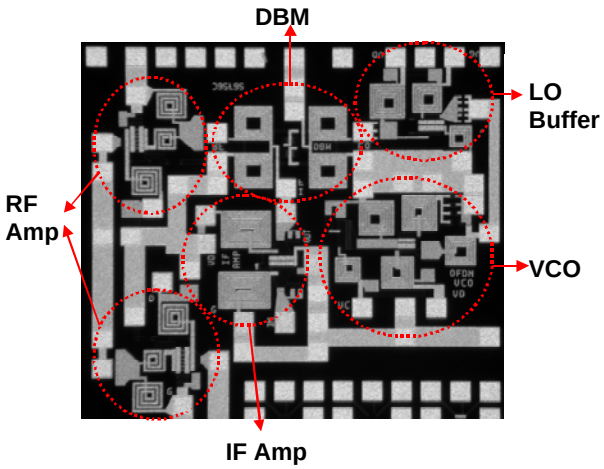



**Figure 13 Photo of the integrated MMIC upconverter chip**

## 4. Conclusion

We have presented RF modules developed based on the SOP concept. The examples demonstrate the advantages of applying SOP approaches to address the present issues of the RF designs. We first presented a 2.4 GHz SiGe HBT power amplifier module and a harmonic suppression filter implemented in LTCC substrate. A C-band transmitter module incorporating an integrated BPF and PA and up-converter MMIC and MLO technology has been presented. Also, a C-band oscillator with external high-Q inductors built in MLO package. Finally, we have presented a very compact 3D-integration concept, based on two stacked LTCC substrates connected by means of µBGA balls. Characterization of the board-to-board transition and an accurate µBGA ball modeling are reported for the first time in RF applications.

**Acknowledgements**

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