

Integrable Miniaturized Folded Antennas for RFID Applications

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Abstract: Low cost, low profile, and miniaturized size are the most critical factors needed to consider in the design of antennas for RFID applications. In this paper we present two simple folded structures based on integrable packaging processes. The first one is a 3D folded patch implemented on LTCC multilayer technology while the second is a printed folded strip antenna fabricated on RT/Duroid board. The dimensions of the folded patch antenna are approximately $\lambda_0/16 \times \lambda_0/16$ and the maximum length of the folded strip is less than $\lambda_0/10$. Both antennas have a peak gain of 0dBi.

I. INTRODUCTION

Radio frequency identification (RFID) is becoming a hot spot in wireless industry [1]. Using an RFID tag, it is much easier for companies to track their products from manufacturer to consumer. In addition to silicon chips, an antenna must be incorporated to transmit ID information to a wireless receiver. The most important factors involved in the design of RFID antennas are focused on low cost, low profile, and miniaturized size while the bandwidth requirement is less critical (only few kilohertz) [2-3]. One solution for low cost is to take advantage of high-volume production. Therefore the antennas must be designed to be part of the tag, that is, they should be integrable with the tag's circuit board. In this paper, we present two miniaturized antenna structures implemented respectively on LTCC multilayer technology and RT/Duroid board. The maximum size of the antenna structures is less than one tenth of wavelength.

II. OPERATING PRINCIPLE

The structure of a folded shorted-patch (S-P) antenna is shown in Fig. 1. The reason why the above structure is referred as a folded S-P is because we consider this antenna is evolved from a conventional shorted patch, as illustrated in Fig. 2. It is well known that a conventional rectangular patch antenna operating at the fundamental mode has an antenna length of $\sim \lambda_0/2$ (see Fig. 2a). Considering the electric field vanishing around the middle of the patch, we can short the patch along its middle line with a metal wall without significantly changing the resonant frequency of the antenna. Thus we get a S-P antenna with an antenna length of $\sim \lambda_0/4$, as shown in Fig. 2b. Next we fold the shorted patch together with the ground plane, reaching to Fig. 2c. Note that the total electric length of the folded S-P will not change very much, but the practical antenna length has been reduced by a half ($\sim \lambda_0/8$). Finally we add a new piece of the ground plane to the right (the original ground plane has become as the upper patch) and press the folded patch together to form the standard folded S-P antenna as shown in Fig. 2d.

The folded antenna can be integrated with RF circuit board in different ways. In the following sections, we will introduce two miniaturized antenna forms. The first one is a folded patch implemented by taking advantage of the LTCC multilayer technology while the second form is a printed folded strip simply realized in an RT/Duroid board.

III. FOLDED PATCH ANTENNA ON LTCC MULTILAYER TECHNOLOGY

The proposed folded patch configuration is shown in Fig. 2. The folded patches are embedded in a ten-layer LTCC substrate (dielectric constant=5.4, layer thickness =0.1

mm). Note that the LTCC substrate is hidden to clearly show the embedded patches. The lower and upper patches are shorted to the ground plane by rows of vias and via pads. The antenna is probe-fed from the bottom to the lower patch through a microstrip line. The dimensions of the folded patch are 3 mm (length) \times 3 mm (width) \times 1 mm (height).

The antenna was simulated using a TLM-based software: Micro-Stripes V6.0. As shown in Fig. 3, the simulated result for return loss agrees well the measured result, which indicates a resonant frequency of 6.36 GHz. The electrical length of the folded patch antenna at the resonant frequency is approximately $\lambda_0/16$. The patch size is less than 1 cm \times 1 cm even if the resonant frequency is scaled down to the 2.45 GHz (one of the RFID operating frequencies). The radiation pattern of the folded patch antenna is plotted in Fig. 4. The peak gain of the antenna is about 0 dBi and the radiation efficiency is 35%. The lower efficiency of the antenna is attributed to its very small electrical size.

IV. FOLDED STRIP ANTENNA ON RT/DUROID BOARD

As shown in Fig. 5, the printed folded strip antenna is fabricated on an RT/duroid 5880 board (dielectric constant=2.2, loss tangent=0.001, thickness=0.508mm). The antenna dimension is 30 mm (width) \times 7 mm (height). The width of the strip lines is 1 mm. The lower and upper folded strip lines are separated by a 0.5 mm-wide slot. The antenna can be matched to a 50-ohms microstrip line by adjusting the position of the feeding point along the lower folded strip.

The simulated and measured results for return loss are compared in Fig. 6 and good agreement is observed. The resonant frequency is about 1 GHz (the antenna electrical size is less than $\lambda_0/10$ at this frequency) and the bandwidth for the 10-dB return loss is 10 MHz (1%). The radiation pattern is shown in Fig. 7. The peak gain is about 0 dBi (radiation efficiency =45%).

V. CONCLUSION

A folded patch and a folded strip antenna are presented in this paper for RFID applications. The folded patch antenna is implemented on LTCC multilayer technology and has a miniaturized antenna size of $\lambda_0/16$. The printed folded strip antenna is fabricated on an RT/Duroid board and the maximum length of the antenna is less than $\lambda_0/10$. Both antennas have a peak gain around 0 dBi and the bandwidths are wide enough for RFID applications. The antennas presented have a planar structure, thus, integrable with RF circuits.

Acknowledgement

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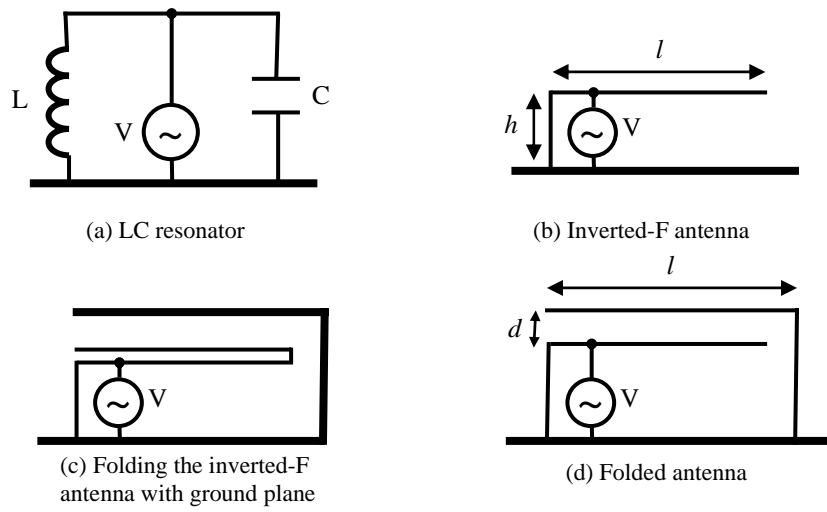


Fig. 1. Development of a folded antenna.

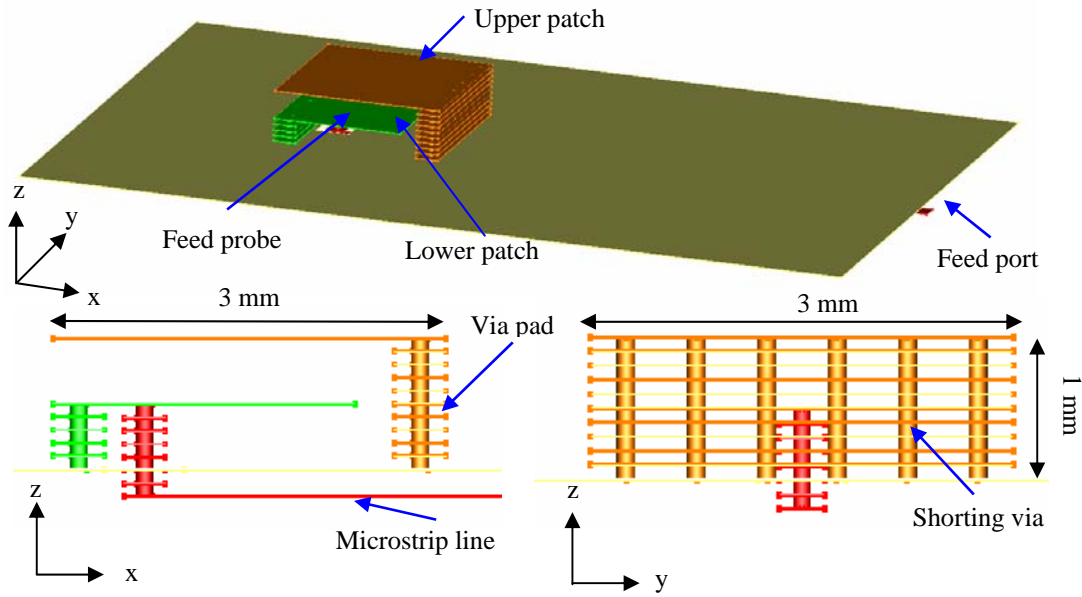


Fig. 2. Folded patch antenna on LTCC multilayer technology.

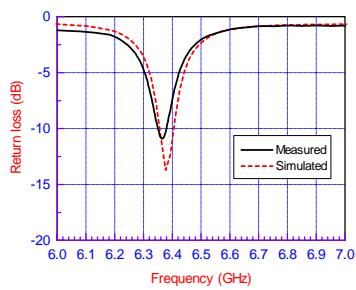


Fig. 3. Return loss of the folded patch antenna.

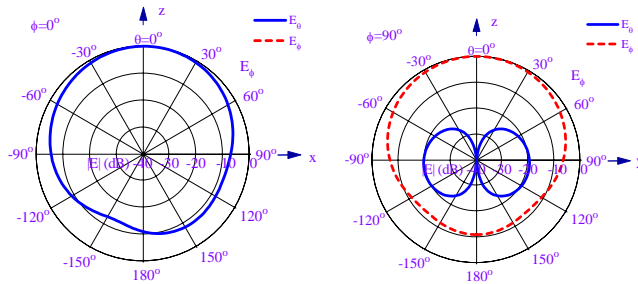


Fig. 4. Radiation pattern of the folded patch antenna.

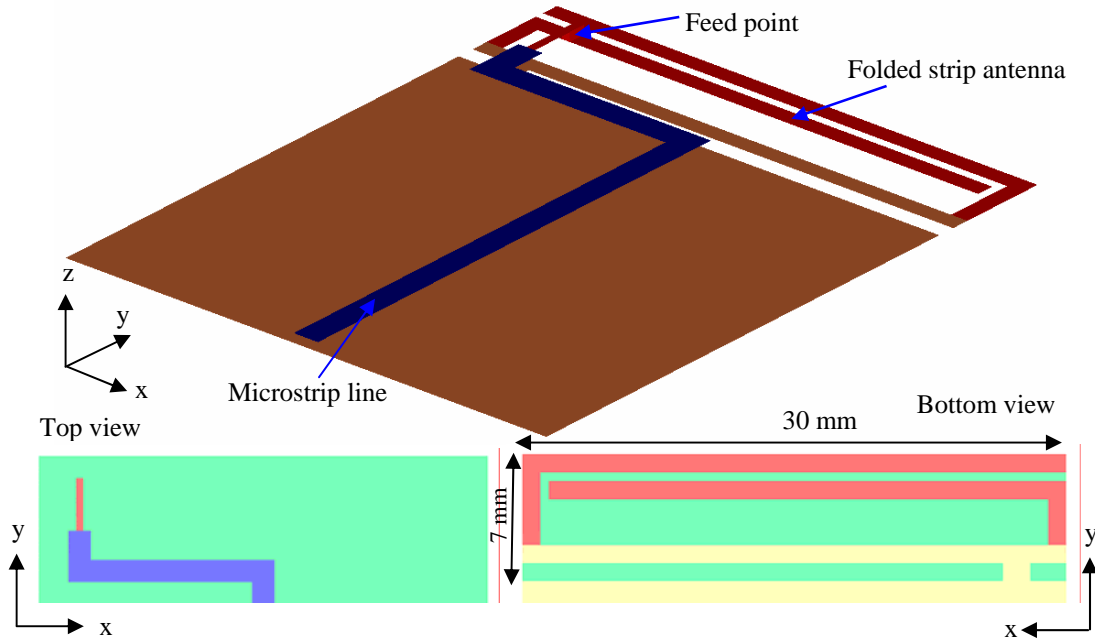


Fig. 5. Folded strip antenna on RT/duroid board.

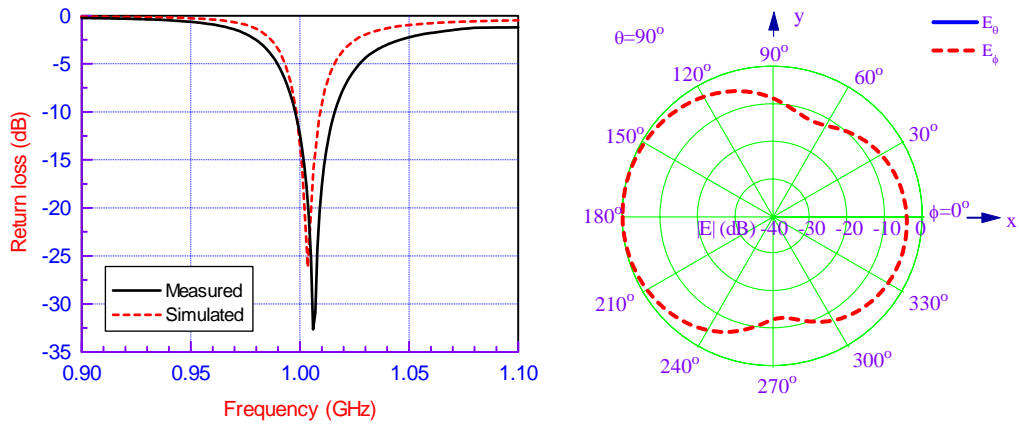


Fig. 6. Return loss of the folded strip antenna.

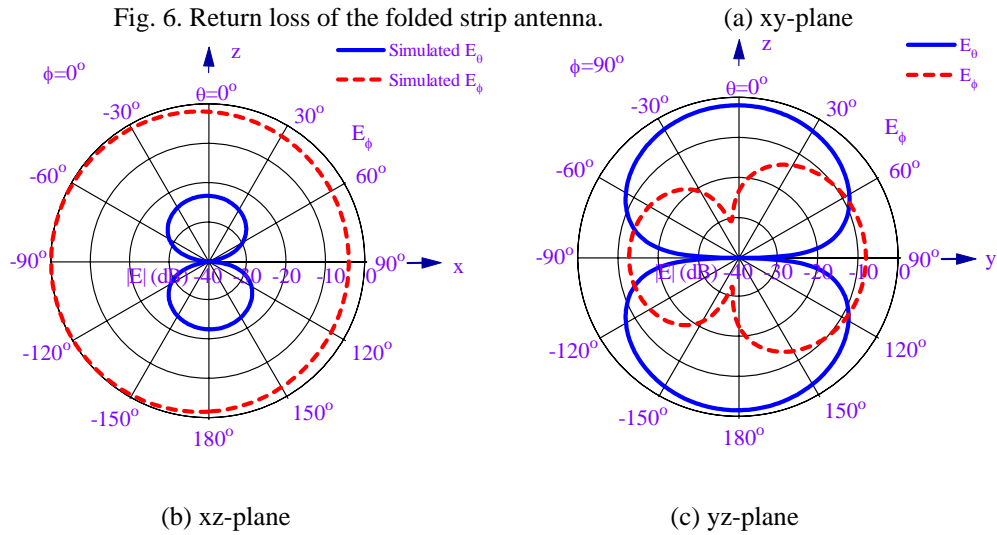


Fig. 7. Radiation pattern of the folded strip antenna.