A Non-Interruptive Link-Variation Monitoring Circuit for Wireless Sensor Applications

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***Abstract*—As wireless sensor devices are usually deployed where the operating environment changes unpredictably, the ability to evaluate the variation in the wireless link is required for reliable and efficient operations. In this paper, a novel link-variation-to-digital-converter (LDC) that provides real-time assessments on the link variations is proposed. Due to its unique structure, the proposed LDC can adjust the resolution of the output data and does not interrupt the original system functionality. A wireless power receiver prototype with a proposed circuit is implemented in CMOS 0.18 μm with an active area of 500 μm-by-20 μm. Measurements of the prototype show that link-variations due to mismatches in the resonant matching condition as well as physical misalignments can be successfully evaluated with the proposed LDC.**

***Index Terms*—Adaptive matching, link variation, resonant matching, wireless power transmission.**

I. Introduction

ADVANCED CMOS technology has enabled integration of multiple functions in a single-chip device that can still maintain reasonably low-power as well as low-cost. With these remarkable accomplishments, the concept of ubiquitous sensing and wireless communication with a micro-scale sensor device was introduced to military, commercial, as well as medical applications [1], [2]. Depending on applications, the core functional blocks of sensor devices are designed to observe different kinds of physical phenomenon such as pressure, brightness, and temperature, and it is highly desirable to maximize the system efficiency of the core blocks. However, the efficiency upper bounds cannot promise consistent performance because a wireless sensor device must undergo variations in the operating environments as the device is deployed. For example, changes in either the physical distance or orientation would attenuate or intensify incoming and out-going signals. Consequently, unless these inevitable yet unpredictable link variations are properly evaluated and compensated, a wireless sensor device would consume unnecessary energy for a given task or too little energy to meet the requirement.

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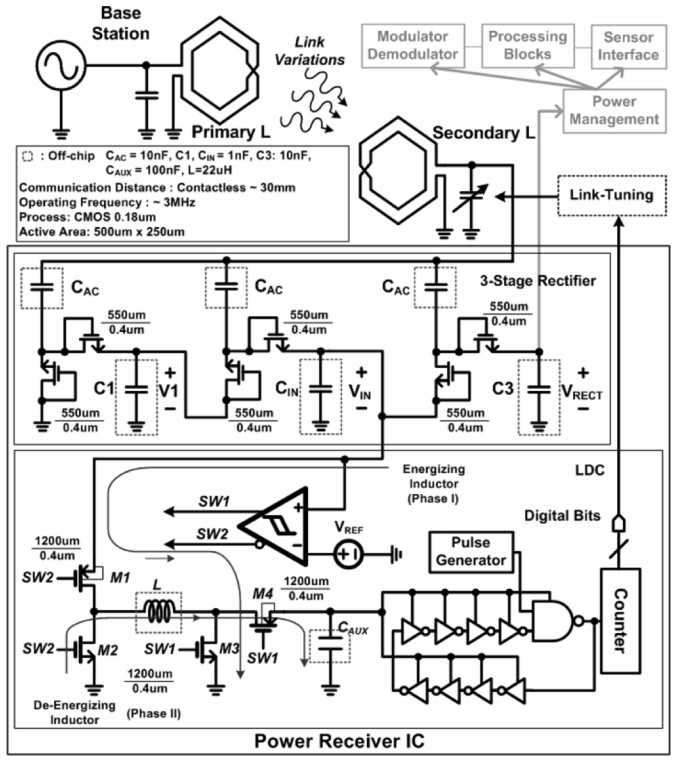

Fig. 1. Block diagram of a tunable power receiver prototype with the proposed LDC in an inductively coupled wireless sensor system.

In [3]–[5], adaptive link-compensating schemes have been proposed. However, in [3], [4], results feature a fixed resolution determined by the physical size of the capacitor bank, and data/power transmission must be interrupted during compensation, and [5] requires external assessment block for link evaluation.

In this letter, a novel non-interruptive link-variation-to-digital converter (LDC) is proposed for wireless sensor applications. The proposed LDC translates link-variations into digital bits that can be easily exploited in compensating the link variations. A power receiver IC with a proposed circuit is designed and fabricated in 0.18 μm CMOS technology to verify the LDC operation.

II. Proposed Link-Variation-to-Digital-Converter

Fig. 1 shows the block diagram of the proposed LDC attached to a conventional wireless sensor device, which often includes a modulator and a demodulator for communication, a

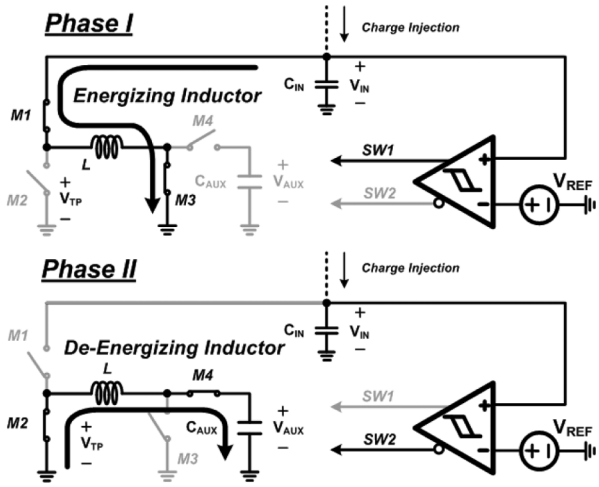

Fig. 2. Operating mechanism of the LDC power chain.

processing unit, a sensor unit, and a power management unit shown in gray solid lines. The link evaluation should have minimal disturbance on the original system functionality, and the outputs are preferred in digital. To achieve these goals, a non-inverting buck-boost power chain and a multi-resolution counting analog-to-digital converter (ADC) have been adopted in the proposed LDC.

The buck-boost chain consists of switches (M1, M2, M3, and M4), an inductor (L), and a hysteresis comparator. When $C_{\rm IN}$ is charged beyond the hysteresis comparator turn-on threshold voltage, Phase I begins as shown in Fig. 2. During Phase I, the comparator closes M1 and M3, and some of the charges in $C_{\rm IN}$ are discharged through L. As L gets energized, $C_{\rm IN}$ loses its charges, and $V_{\rm IN}$ decreases. When $V_{\rm IN}$ is below the turn-off threshold voltage, the comparator opens up M1 and M3 and closes M2 and M4 (the beginning of Phase II). During Phase II, the previously energized L dumps its remaining magnetic charge to $C_{\rm AUX}$. When $V_{\rm IN}$ charges up beyond the switching threshold, Phase II ends, and Phase I repeats.

As link variations influence the charge flow rate in $C_{\rm IN}$, the buck-boost chain translates the charge flow rate into a ratio of a Phase I duration, $t_{\rm on}$, to a Phase II duration, $t_{\rm off}$; since the charge injection originates from the voltage multiplier, the sum of the two duration stays constant. From the principle of inductor volt-second balance [6], we can see that $V_{\rm AUX}$ is strongly correlated with link-variations

$$\frac{V_{IN}t_{on}}{L} = \frac{V_{AUX}t_{off}}{L} \rightarrow V_{AUX} = \frac{t_{on}}{t_{off}}$$
$$V_{IN} = \frac{D}{1-D}V_{IN} \quad (1)$$

where $D = t_{\rm on}/(t_{\rm on}+t_{\rm off})$ and $V_{\rm IN}$ is proportional to the charge flow rate.

The digitizer in the LDC is realized with a ring oscillator and a digital counter. The supply of the oscillator, which consists of eight inverters and a NAND for an enable function, is connected to $V_{\rm AUX}$. The oscillation frequency is proportional to $V_{\rm AUX}$, and the counter converts the frequency into a digital code that represents the strength of $V_{\rm AUX}$. The counting duration is controlled by the width of a pulse from the pulse generator. This duration determines how much energy should be invested for the link-evaluation; a longer period of counting can result in a finer resolution.

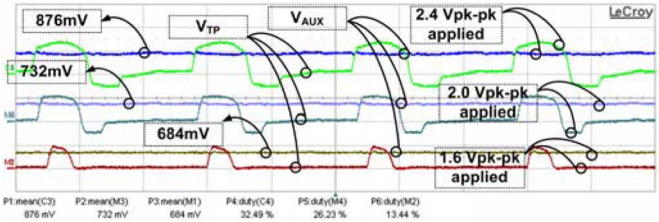

Fig. 3. Duty cycles and power chain output voltages for 2 MHz input AC amplitudes of 2.4, 2.0, and 1.6 Vpk-pk applied to the power receiver.

III. Tunable Power Receiver Prototype

The tunable power receiver prototype consists of an off-chip tunable L-C network, a three-stage rectifier, and a proposed LDC block. The L-C network is realized with a flexible printed circuit board (FPCB) inductor and film-trim capacitors. The FPCB inductor was designed to have Q-factor above 100 and inductance of 15 μH. The physical dimension of the FPCB inductor is about 45 mm $\times$ 45 mm. For the prototype verification, the same FPCB inductors are used for the primary and the secondary coils. The three-stage rectifier is implemented with diode-connected transistors and forms the main energy path.

The amount of dc energy harvested at C3 will be affected by the link-variations in the inductively coupled link; mismatches in the resonant matching networks and inductor misalignments would be major cause for the link-variations. Therefore, with the power receiver prototype, realistic link-variations can be emulated and the functionality of the proposed LDC can be tested. Since the buck-boost power chain in the LDC isolates the remaining evaluation blocks from the main energy path, the input energy can be continuously harvested even during the link-evaluation. After the evaluation, the LDC is disabled, and the evaluation results are applied to the link-tuning operation in which a simple binary algorithm adjusts the off-chip tunable capacitor banks.

IV. Measurements

The combination of the FPCB inductors and the capacitor banks has a resonant frequency range of 1–5 MHz. Fig. 3 shows the power chain output, $V_{\rm AUX}$, and the corresponding duty cycle waveforms, $V_{\rm TP}$, for three input amplitudes, 2.4 $V_{\rm pk\text{-}pk}$, 2.0 $V_{\rm pk\text{-}pk}$, and 1.6 $V_{\rm pk\text{-}pk}$, applied to the prototype. As 2 MHz signals are applied to the receiver with pulse periods of 2.5 μs, 5 μs, and 10 μs, the rectifier output, $V_{\rm RECT}$, and the LDC outputs are plotted in Fig. 4. The higher counting period is, the finer input amplitude can be differentiated.

To verify the link-evaluation capability under component mismatches, a 2 MHz signal is transmitted through a fixed primary resonant network to a 2 mm-away secondary resonant network, and the rectifier voltages and the LDC outputs are measured with various tuning capacitor values in Fig. 5. To emulate realistic inductor misalignment situations, the proposed

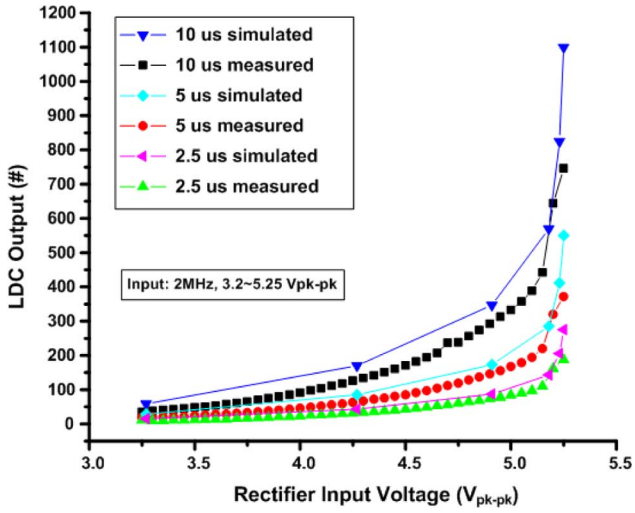

Fig. 4. LDC outputs when 2 MHz sinusoidal signals with 3.2–5.25 $V_{pk\text{-}pk}$ are applied to the input of the rectifier.

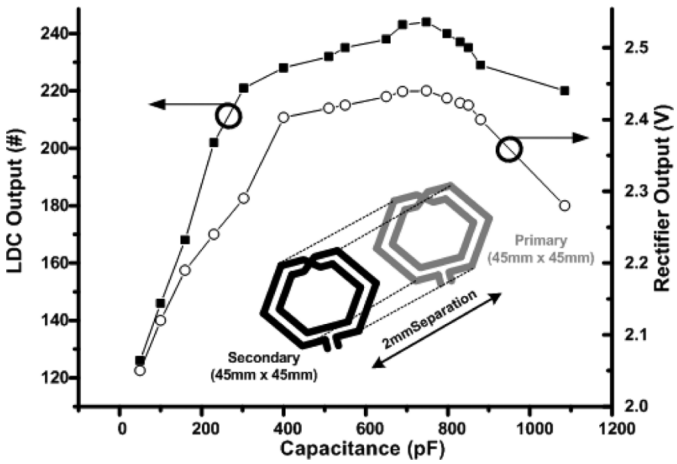

Fig. 5. Tuning capacitance value versus LDC digital outputs and corresponding rectifier output voltages.

power receiver was tested with five different inductor alignments. While the coordinate of the primary inductor is fixed, the secondary inductor is offset by 2 mm distance in either/both X-direction and Y-direction. For the inductor misalignments, the LDC outputs are measured with various capacitor values, as shown in Fig. 6.

The active area of the prototype, implemented in CMOS 0.18 μm, is 500 μm-by-250 μm. Fig. 7 shows the die photo of the prototype and an inductor misalignment that has been tested.

V. Conclusion

In practical wireless sensor applications, unpredictable variations in the wireless link inevitably degrade the overall system performance. Evaluating the link variations in real-time is highly desirable for more reliable and efficient operations. This work presents a unique non-interruptive link-variation sensing technique that can provide *in situ* multi-resolution assessments.

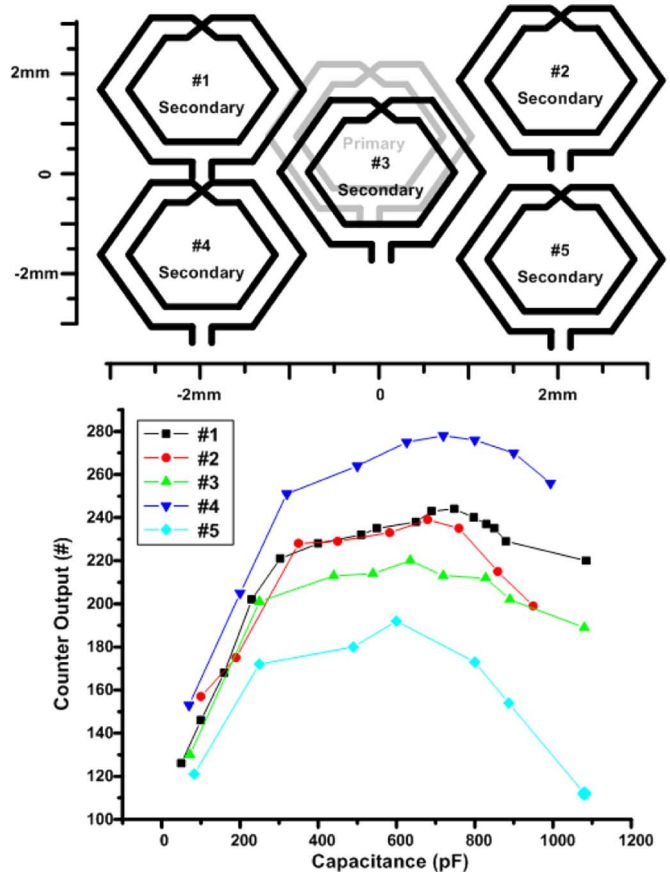

Fig. 6. Tuning capacitance value versus LDC digital outputs under various inductor misalignments.

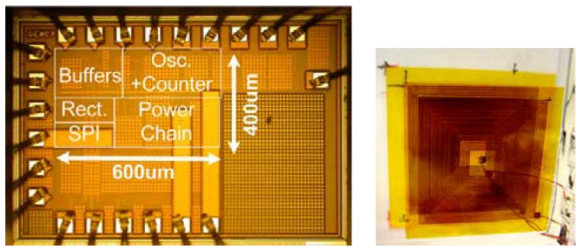

Fig. 7. Die micrograph of the power receiver prototype and an example of an inductor misalignment.

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