State-of-the-Art Inkjet-Printed Metal-Insulator-Metal (MIM) Capacitors on Silicon Substrate

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***Abstract*—Vertically-integrated metal-insulator-metal (MIM) capacitors on silicon are demonstrated for the first time utilizing an entirely additive RF-specific inkjet-printing process. The inkjet-printed MIM capacitors demonstrate a high capacitance per unit area of up to 33 $\mathrm{pF/mm^2}$ by utilizing novel dielectric inks, while achieving quality factors (Q) up to 25 and self-resonant frequencies (SRFs) above 1 GHz. Measurements of dielectric permittivity, leakage current, voltage breakdown, and fabrication repeatability are presented confirming the high-performance operation of the printed MIM capacitors.**

***Index Terms*—Inkjet-printing, printed electronics, RF passives, silicon, thin-film capacitors.**

I. Introduction

THE ever-increasing miniaturization of silicon-based electronics is creating new challenges for packaging technologies which need to reduce overall package size, parasitics, and cost, all while allowing for design flexibility and manufacturing reconfigurability. Traditional packaging technologies which utilize flip-chip or wire-bond chip integration with ICs, such as LCP or LTCC, are utilized to integrate components which are either too large to fabricate on-chip, require higher performance than obtainable on lossy silicon, or contain non-CMOS compatible materials such as sensing films. Inkjet-printing has recently demonstrated the ability to package vertically-integrated components including MIM capacitors, mm-Wave antennas, and sensors in a rapid, low-cost, additive, and substrate-independent manner [1]–[4]. While vertical printing technologies have yet to demonstrate RF components on silicon, directly printing components on-chip to create a wafer-scale package, that does not require flip-chip or wire-bond interconnects, presents major advantages in manufacturing cost, simplicity, and parasitics reduction. This work demonstrates the first vertically-integrated components packaged on top of silicon. Through the optimization of the vertically-integrated printing process and the formulation of novel higher-permittivity thin-layer dielectric polymer inks, MIM capacitors with improvements of over 50% in per square area capacitance and 300% in quality factor over prior art in the literature, for inkjet printed devices are demonstrated [3], [5]–[8]. The goal of this work being to prove the reliability of inkjet printing and traditional technologies combination.

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TABLE I
Silicon Substrate Properties From University Wafer

Parameter	Value
ID	1706
Type	Undoped
Diameter	76.2 mm
Resistance	1000 Ω-cm
Thickness	380 μm
Polish	Double-sided

II. Fabrication: Materials and Process

Silicon is an inherently difficult substrate to print on as both silicon and its various oxidation states have surface energies which yield poor wetting [9]. In this section, the materials and methods used to define a silicon-specific process for vertically-integrated RF electronics are presented.

A. Materials

The characteristics of the silicon wafer utilized (Product No. 1706, University Wafer) are displayed in Table I. A pre-treatment layer, which has the functions of forming a printable surface for subsequent layers and isolating the MIM capacitor from the lossy silicon, is printed utilizing an ink containing 35 w/w% SU-8 short-chain polymer in a cyclopentanone solvent (MicroChem, Newton, MA), which deposits 6.5 μm thick layers per pass (considered thick for inkjet printing). The conducting metal layers are printed utilizing Cabot CCI-300 silver nanoparticle ink (Cabot Corp., Boston, MA) which contains 20 w/w% silver nanoparticle powder in an ethanol/ethylene glycol solvent which forms 500 nm thick layers per pass (considered thin for inkjet printing). The thin-film dielectric layers are deposited utilizing two different dielectric inks which contain 1:10 and 1:1 w/w% ratios of poly(4-vinylphenol) (PVPh), a long-chain polymer (Product No. 436216, Sigma Aldrich), and poly(melamine-co-formaldehyde) (PMF), a heat activated crosslinker (Product No. 418560, Sigma Aldrich) in a 1-Hexanol solvent which form 800 nm thick layers per pass. The variation of the ratio of PVPh to PMF allows for tuning the permittivity (ε_r) and loss tangent ($\tan\delta$) of the deposited thin-film layer. The characteristics are summarized in Table II.

TABLE II
RECIPES (RATIO BY WIGHT) AND CHARACTERISTICS FOR THE PVPH-BASED INKS; THE THICKNESS IS RELATIVE TO 2 PRINTED LAYERS

Ink	PMF	PVPh	Hexanol	ε_r	tanδ	Thickness
1	0.5 %	5 %	94.5 %	3	0.04	1.6 μm
2	2 %	2 %	96 %	5.5	0.03	1.8 μm

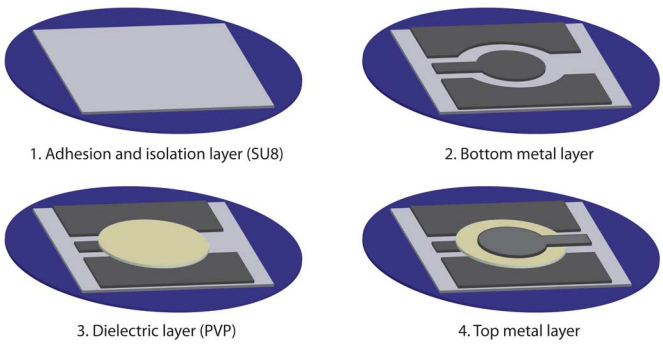

Fig. 1. Fabrication process description.

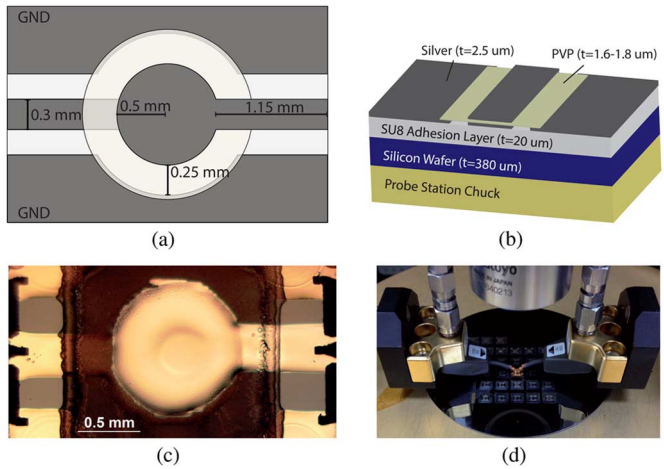

Fig. 2. Capacitor simulation model: (a) top view, (b) cross sectional stack-up, (c) optical micrograph of MIM capacitor, and (d) MIM capacitor test setup. Note that the little spreading effect of the PVPh, visible in (c), is not affecting the performance of the devices and it is present only at the edges of the pattern.

B. Process

The process (Fig. 1) utilizes the Dimatix DMP-2800 printing platform with 10 pL nominal drop volume cartridges. After cleaning the wafer, three layers of SU-8 ink are deposited to form a 20 μm (enough to ensure isolation from the silicon) passivation layer with an average surface roughness of 53 nm. The SU-8 is then cured utilizing a pre-exposure bake at 90°C for 5′, 365 nm UV exposure, and a post-exposure bake at 120°C (10′). Following curing, a 30 s UV-Ozone exposure is performed to increase the surface free energy of the SU-8 from 30 to 40 mN/m for optimal wetting. Note that SU-8 has been chosen as it is, "thick" and easy-to-print on silicon, thus allowing the fabrication of fully inkjet printed devices. Subsequently, five layers of silver-nanoparticle ink are deposited and dried in the oven at 120°C to form a 2.5 μm thick metalization. A UV-ozone exposure of 2′ is then performed to increase the surface energy of the SU-8 back to 40 mN/m for the effective printing of thin-film dielectric. Two layers of the PVPh dielectric ink are then printed and cured at 180°C on a hotplate for 10′. Finally, five layers of silver are printed (no UV-Ozone exposure is performed before this step) to form a 2.5 μm thick top metal layer and the entire structure is cured in the oven at 180°C for 1 h. It is important to clarify that, by curing each film before printing the next one, there is no dissolution between layers of different materials. Moreover, during the entire process the drop space of the printer is set to 20 μm.

III. DESIGN AND SIMULATION

The MIM capacitors are simulated utilizing the Computer Simulation Technology (CST) Microwave Studio frequency domain solver. The geometry of the MIM capacitors is reported in Fig. 2(a). The capacitive plates have a radius of 500 μm and are fed by CPW lines having a center conductor width of 300 μm and a gap of 250 μm. The cross sectional view in Fig. 2(a) illustrates the material stack-up used in the 3-D model which includes the Brass probe station chuck. The silicon wafer has $\varepsilon_r = 11$, $\sigma = 0.1$ S/m and a thickness of 380 μm. The SU-8 passivation layer has $\varepsilon_r = 3$, $\tan\delta = 0.04$ [10], and a thickness of 20 μm. The silver nanoparticle layer has $\sigma = 5\text{E}6$ S/m and a thickness of 2.5 μm [11]. The 1:10 and 1:1 ratio PVPh dielectric layers have $\varepsilon_r = 3$ and 5.5, $\tan\delta = 0.04$ and 0.03, and thicknesses of 1.6 and 1.8 μm, respectively. These values are computed inverting the MIM capacitance equation and refining the materials model with a post-measurement processing.

IV. RESULTS

The fabricated MIM capacitors are shown in Fig. 2(c) and (d). To measure them, the wafer is probed utilizing ACP-GSG-500 probes with an Anritsu 37369A VNA. Fig. 3(a) reports the capacitance versus frequency of MIM capacitors fabricated with 1:10 and 1:1 ratios of PVPh and PMF. Two different runs are shown to demonstrate the repeatability of the process. The MIM capacitors fabricated with a 1:10 ratio of PVPh to PMF have a measured capacitance of 12 pF or 15.8 pF/mm^2, a maximum Q of 22, and a SRF of 1.2 GHz. The MIM capacitors fabricated with a 1:1 ratio of PVPh to PMF have a measured capacitance of 25 pF or 33 pF/mm^2, a maximum Q of 25, and a SRF of 0.9 GHz. Both the measurements agree well with the predicted full-wave simulation results (Fig. 3). The repeatability of both the capacitance value and Q for both ink variations are within 5%, which demonstrates the reliability of the vertically-integrated inkjet-printing process proposed in this work. An important point to highlight is that the Q values reported in this work are over three times higher than prior results of printed MIM capacitors which were fabricated on a lower-loss substrate [3], [8], see Table III. This achievement is the result of combining a refined geometry, a smoother substrate (compared to kapton in [3], for instance) and the improvement of PVPh printing process. The leakage current and breakdown voltage are measured with a Keithly 6487 pico-ammeter. The results (Fig. 4) display the leakage current versus applied voltage up to 50 V. The leakage current has a log-linear trend which is typical of thin-film MIM capacitors, with a maximum of 40 pA/mm^2

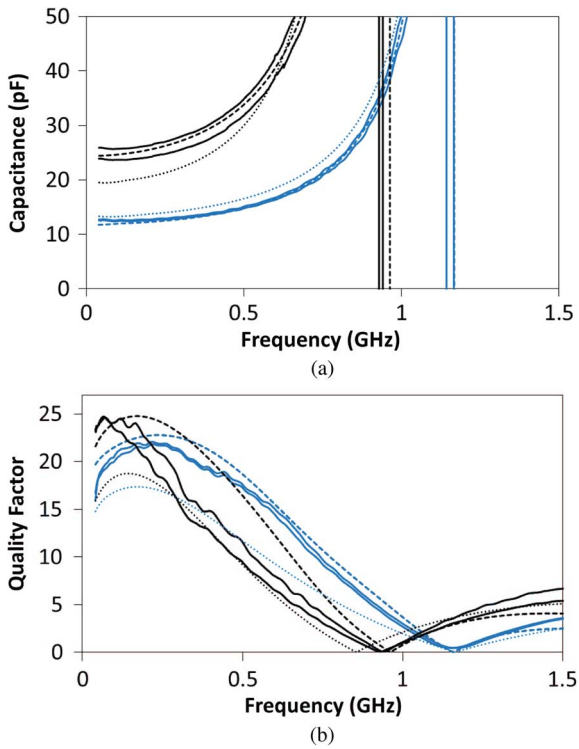

Fig. 3. Simulations (dashed line) versus measurements of two prototypes per ink (solid line): (a) capacitance (C) in pF, and (b) quality factor (Q). Each test has been performed at frequencies ranging from 0.4 GHz to 2 GHz. Ink 1 is in blue while ink 2 in black. Simulation (dotted curves) with a lossy-silicon substrate are also included to demonstrate the effectiveness of the passivation layer.

TABLE III
COMPARISON WITH THE STATE-OF-THE-ART

Ref	SRF	max Q	C/area
[3]	3 GHz	7.5	22.2 pF/mm^2
[8]	2.5 GHz	–	8 pF/mm^2
this work	1 GHz	25	33 pF/mm^2

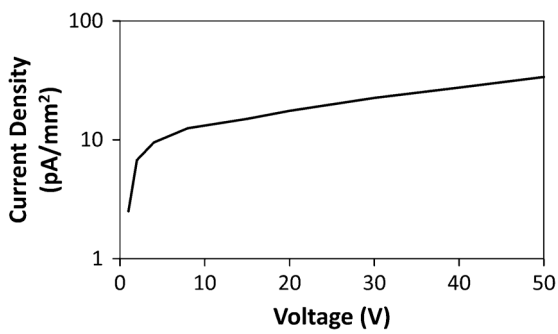

Fig. 4. Leakage current density J $(\mathrm{pA/mm^2})$ measurement (log scale) with applied voltage ranging from 1 V to 50 V.

at 50 V [12]. Above 50 V the PVPh film tends to break down and short.

V. CONCLUSION

The MIM capacitors presented in this work are the first ever fully inkjet-printed passive components on silicon wafer. A vertically-integrated printing process has been outlined which utilizes a printed SU-8 passivation layer ink to improve ink adhesion and allow for printing on silicon which has previously been a difficult task due to the unfavorable surface energy of silicon and silicon oxide. As part of the vertically-integrated process, two PVPh thin-film dielectric are created, with 1:10 and 1:1 ratios of PVPh polymer to PMF crosslinker, yielding permittivities varying from 3 to 5.5. Two 0.5 mm-radius circular MIM capacitors have been fabricated obtaining C equal to 12 pF (ink 1) and 25 pF (ink 2). Printed MIM capacitors demonstrated utilizing the same vertically-integrated process, however with two separate PVPh dielectrics, have maximum capacitances of 33 $\mathrm{pF/mm^2}$, SRFs of 1.2 GHz, and most importantly maximum Qs of over 25 which is more than 300% higher than previously reported inkjet-printed MIM capacitors with similar capacitance values. The capacitors show extremely low leakage currents and a high voltage breakdown, above 50 V. The results demonstrate a major improvement on inkjet-printed passive components and open the door to a new packaging methodology in which additive inkjet-printed electronics and traditional circuits can be combined to reduce cost and packaging complexity, and introduce a new level of flexibility to the packaging process.

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