Flexible LCP and Paper-based Substrates with Embedded Actives, Passives, and RFIDs

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Abstract

Miniaturization with increased functionality at reduced cost historically has been the key driver for the evolution of electronics products. However, the size reduction was traditionally confined to lateral dimensions, until recently in the 21st century, the real estate in the Z-direction has been severely compromised, therefore, THIN has become the buzz word encompassing thin die, thin dielectric, thin passives, thin core and ultimately leading to thin packages. This paper overviews the trends from thick to thin electronic products, materials, processes, and manufacturing of the thick and thin packages with embedded passive components such as resistors, capacitors, inductors, and lately the Actives. Flexible organics with embedded IC and thin film passive materials and substrates that can perform at frequencies in the range 2-110 GHz has been established with liquid crystal polymers . A roadmap for the realization of highly integrated RFID tags with wireless sensors and thin film batteries on ULTIMATE low-cost synthetic material such as photocopy papers has been addressed. To this regard, special attention is given to miniaturization of antennas and on specific techniques for ultra-high-efficiency (95%) RFID's. Examples of paper-based conductive Ink-Jet printed circuits as well as copper circuitary by etching have been investigated as a means for further cost reduction including ultra-thin printed batteries and power-scavenging devices, as well as to miniaturized sensors (temperature, chemical, pressure) that would enable long-range ubiquitous sensing. Dielectric constants and dielectric loss measurements on paper-substrates are reported for the first time at frequency >1GHz.

Keywords

RFID, Paper-Substrate, Ink-Jet Printing, Antenna, LCP, Embedded Active, Embedded Passives.

Challenges in Embedded Actives

The semiconductor industry has faced with a tremendous growth in functionality, increased speed and performance and reduced cost. The advances in photolithography have provided latitude in keeping up with the consumer demands in miniaturization and portability of consumer electronics products. With the increased level of interconnections and flexibility in System-in-Chip and System-on-Package, the size of the device is becoming more often the size of the circuit board than anything else. So, the next question is how to reduce the size of the circuit board – the likely answer is of course with embedded components. Although embedded passives have received attention in the industry over the past 5 years, the net effect in miniaturization with embedded passives is not yet significant due to inherent materials constraint with targeted need for replacement of discrete components, e.g., capacitors with capacitance density greater then 1 $\mu F/cm^2$. Table 1 shows the Roadmap for embedded components in the consumer market share emphasizing the need for embedding passives as well as active components [1].

Since the inception of GE's chip first process, several approaches have been undertaken in the past 5-10 years for embedding chips into polymer and other core matrices including PWB. Notables among these processes are Fraunhofer IZM chip in polymer, Imbera chip in board, European Commission's Hiding Die Project, Matsushita SIMPACT, and Intel's embedded discretes. However, the basic approaches can be simplified by four major categories [1] as depicted in Figure 1. The major challenges for embedding actives are thermal managements, reworkability, and mechanical robustness. Question now is whether reduced package size and reduced interconnect loss can justify implementation of actives – a similar scenario which is being faced today when selecting embedded passives vs SMT components. An analysis of parasitics in different package configuration was conducted by Daum showing HDI with embedded components and actives could lead to a significant reduction in R, L, C parasitics [2].

Table 1. JAPAN's View of Embedded Technology [1]

Products	2006	2008
Wearable products	R, Filter	L
Portable Audio Player	R, L, Filter	C
Cell Phone	Memory, Logic	Linear
PDA	Memory, Logic	Linear
Digital Still Camera	R, L, C. Filter	Memory, Logic, Linear
Digital Video Camera		Memory, Logic, Linear
Notebook PC	L	
Car Entertainment System	C, R, Filter	L,Memory, Logic, Linear
Engine Controller	R	C, L, Filter,
Digital TV and Set Box	C, L, R, Filter	Memory/ Logic/Linear
High End Server/ Computer	C, L, R, Filter	

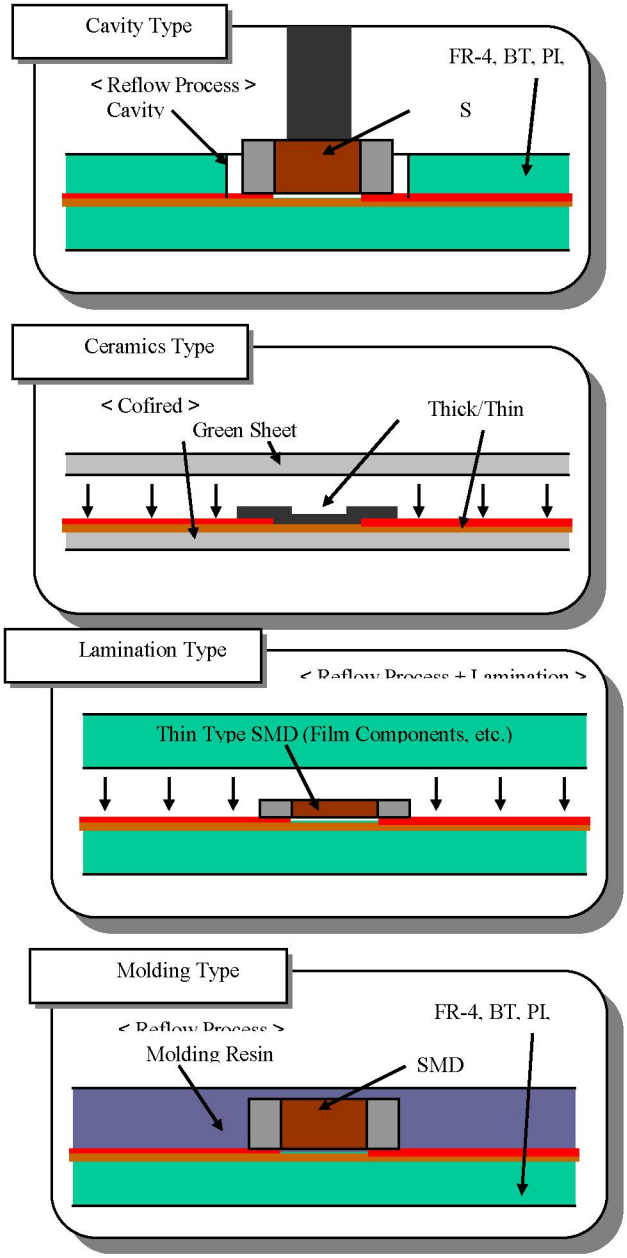


Figure 1. General Approaches for Embedding Actives.

Challenges in Embedded Passives

There are numerous challenges in manufacturing embedded passives, some of them are discussed briefly [3].

Mixed Signal Design Tools:

There are two issues with the design. First is the layout and artwork generation and second is performance simulation. Most buried resistors can be shaped and located according to simple design rules, however, CAM station automated design rule check software is limited to checking minimum size and clearances around the buried object. The lack of CAD/CAM systems with electrical modeling and simulation capability is a major obstacle to using embedded passives for frequency sensitive applications as cost and time-to-market considerations restrict "trial and error" designs iterations. Companies that have implemented embedded components have been forced to develop their own design tools. The design tool companies appear to be waiting for the technology to take off before they get actively involved. This impedes a large scale adoption of the technology. Industry that has the need to design for high speed in copper will be required to continue to manually design and place embedded component. This may end the "chicken and egg" stalemate that has existed for the last few years. The ability to achieve better than 1% precision values is critical in new high-end systems (i.e. super servers and workstations) that are pushing data bus performance approaching >2GHz clock rates. In these systems the resistor must be nearly "ideal" and must accurately match the impedance of the trace on the board to prevent signal reflection and ensure clean signal integrity. Modeling is becoming more important as speeds increase and board designs become more sophisticated. Many design centers are just beginning to experience the need for termination. There is a distinct lack of information on terminations and the related issues in the integration of the design process, i.e. integrating logic, signal integrity, EMI, and PCB design.

Better Embedded RC Materials

Polymer thick film (PTF) can have high resistivity but have poor tolerance, especially stability over time. Thin film materials have good stability but only low resistivity and only fair tolerance. Thus, no materials exist with high resistivity values and good stability. Material development is critically needed for applications requiring higher R values (which most mobile products require) and tighter tolerances than 10%. TCR is also an important parameter which needs to be lower than 50ppm/C which is not currently available for the higher resistance values.

Embedded capacitors are much more sensitive to their environment than resistors (e.g. frequency dependency, board resonance). They also serve a wider variety of functions (e.g. decoupling, by-pass, tuning, filtering, converting, protecting). There certainly exist technical barriers and challenges in embedded thin/thick film passives for other companies and institutes worldwide. It is due to difficulties in materials, processes and manufacturing technologies in general. Also, not just single, but multiple solutions of material and process are needed to cover RF and decoupling capacitance ranges and parameters.

Defect Free Manufacturing

Many new materials under consideration require processes new to circuit board fabricators (e.g. screen printing) and some require processes not done anywhere presently (e.g. laser trim on FR4). Well-defined areas, thickness control and achieving tight tolerances are critical needs to the manufacturing process. Yield loss per device must be extremely small (~0.0001) because integral resistors cannot be repaired. Multi-layer structure with embedded passives requires different materials – it's necessary to have them processed without significant deviation in tooling.

Higher Power Densities

The power density of the available materials is rated at 10W/in^2 or more, which is adequate in the near term. As densities increase, this may become inadequate.

Rapid Prototyping

Rapid Prototyping is perhaps the most serious bottleneck, for example, the turnaround time for a revision of resistor values and placement must be 3 days!

Test and re-workable during and after assembly

Production yield depends on soundness of design, materials and precision manufacturing, etc. However, finding methodology to sort out any failure effectively during and after manufacturing is another challenge and barrier especially when components are embedded instead of surface mounted. For this, a so-called BIST (Built-in Self Test) technology in which a self test circuit is implemented in the system with embedded components to monitor manufacturing and final functionality of the system will be required. Re-workability of embedded components in the middle of process is also challenging task and should be a barrier. This is directly related to yield and should be minimized by strict process control, similarly done in CMOS and LTCC processes.

Reduce Layer Count

As the number of layer increases, each layer becomes progressively more expensive than the preceding layer since significant investment has already been made to complete fabrication of the preceding layers. It is imperative to come up with materials and processes particularly for R, L, and C within the same layer, thus reducing the layer count and decreasing the cost. The RLC in a single layer is currently being investigated. A process flow for three different approaches is outlined below:

Approach 1

(a) Deposit polymer/ceramic composite dielectric such as epoxy/barium titanate on copper foil and partially cure to B-stage polymer
(b) Sputter a thin resistive film such as NiCr on a Cu foil
(c) Laminate (b) on (a) with resistive film in contact with the polymer/ceramic dielectric
(d) Remove Cu and resistive layer on undesired area by chemical etch
(e) Pattern copper to form capacitive electrodes, resistive terminal pads, and inductors thereby completing RLC components in one layer
(f) Pull out terminal pads to another layer for RC or RLC integrated filters or other passive devices

Approach 2

(a) Deposit polymer/ceramic composite dielectric such as epoxy/barium titanate on copper foil and partially cure to B-stage polymer
(b) Sputter a thin resistive film such as NiCr on Cu foil partially covered with a sacrificial polymer
(c) Remove sacrificial polymer which in turn removes the sputtered resistor
(d) Laminate (c) on (a) with resistive film in contact with the polymer/ceramic dielectric
(e) Remove Cu and resistive layer on undesired area by chemical etch
(f) Pattern copper to form capacitive electrodes, resistive terminal pads, and inductors, thereby completing RLC components in one layer. This construction allows capacitors and inductors with only copper metallization opposed to Approach 1 where capacitor and inductors had resistive layer underneath Copper.
(g) Pull out terminal pads to another layer for RC or RLC integrated filters or other passive devices.

Approach 3

(a) Deposit polymer/ceramic composite dielectric such as epoxy/barium titanate on copper foil and partially cure to B-stage polymer
(b) Sputter a thin resistive film such as NiCr on a Cu foil
(c) selectively laminate (b) and pristine copper foil on (a) with resistive film in contact with the polymer/ceramic dielectric
(d) Remove Cu and resistive layer on undesired area by chemical etch
(e) Pattern copper to form capacitive electrodes, resistive terminal pads, and inductors, thereby completing RLC components in one layer. This construction allows capacitors and inductors with only copper metallization opposed to Approach 1 where capacitor and inductors had resistive layer underneath the copper metallization.
(f) Pull out terminal pads to another layer for RC or RLC integrated filters or other passive devices

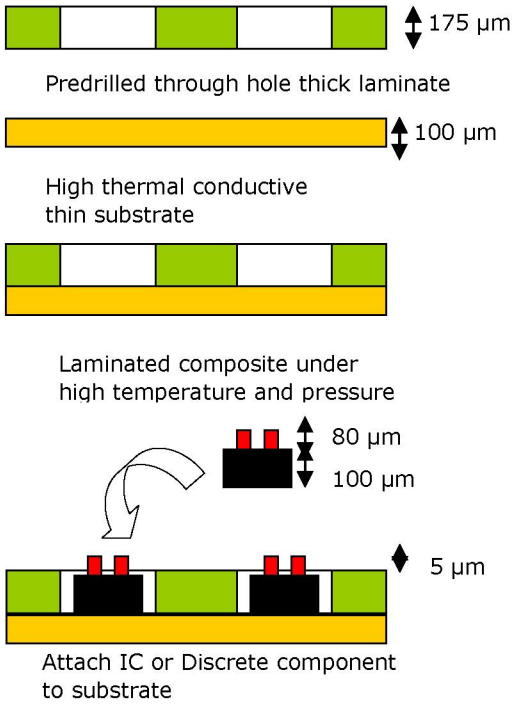
These processes can also be implemented for double sided RLC on a single layer dielectric. Realization of RLC in a single layer will reduce cost significantly with simultaneous reduction in thickness.

Embedded IC and Passives and RFID in LCP

The low loss (tan δ = 0.002-0.005) up to mm-wave frequency range, near hermetic nature (water absorption < 0.04%) required flexible MEMS packaging, and lower cost (projected $5–$7/sq. ft. for large volume production), make LCP appealing for high frequency designs where excellent performance is required for minimal cost. LCP's low water absorption makes it stable across a wide range of environments by preventing changes in the relative dielectric constant (ε_r) and loss tangent (tan δ). Also, LCP is a flexible material which allows for the realization of conformal RF modules in non-orthogonal and non-planar surfaces. LCP can also serve as package and dielectric and sealing for MEMS structures.

Embedding IC

Embedding chips itself within the core in not new, however, there are several barriers for its commercialization. Two important issues are thermal solutions and location of chips within the PCB to prevent damage of the chip in subsequent processing. The authors propose a combined path for embedded chips as well as embedding passives with novel low loss thick and thin film dielectrics to enhance thermal solutions of the embedded IC in a flex circuitary suitable for RF applications in frequency range above 60 GHz (Figure 2). The proposed materials are low loss Liquid Crystal Polymer (LCP) and Benzocyclobutene (BCB). The proposed process scheme



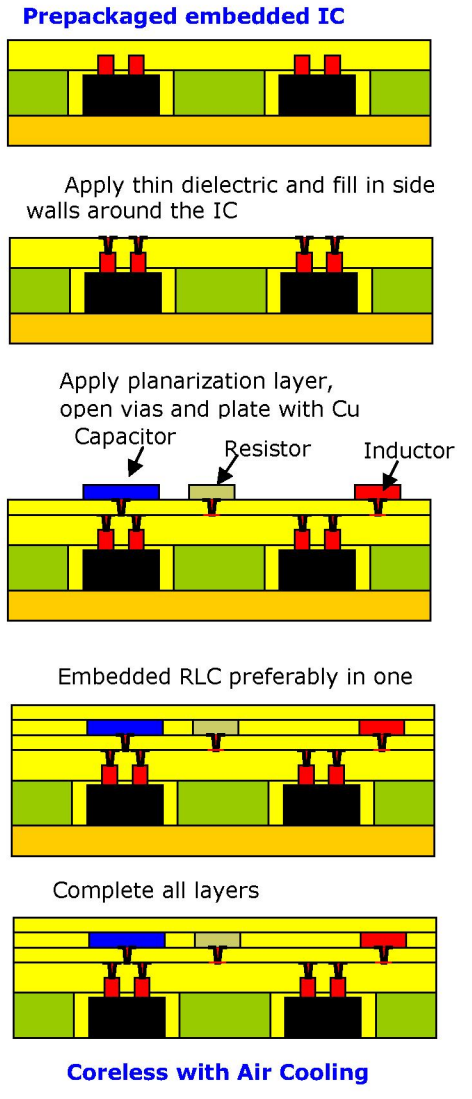


Figure 2. Conceptual IC embedded Process in LCP

is a modification of Torikka [4]. The key advantages in this combined solid LCP/liquid BCB process are:

Embedded chip cavity by mechanical drilling (No laser ablation)
Heat extraction from the top of the chip with high thermal conductive plate or by open air cooling
Co-existence of embedded actives and passives on flex
Coreless packaging
Packaged flex substrate ultra low loss materials (ϵ_r <3, tanδ <0.003)
Direct copper plating on low loss BCB
Electroless plated resistor on BCB
Large format processability
Prepackaged IC
Adjustment of chip height made easy
Cooling with high conductive thin plate superior to copper.

Still the challenges are CTE mismatch, adhesion, and registration. Polymer/Polymer adhesion (LCP to BCB) is expected to be resolved by plasma treatment. The CTE mismatch will be addressed and minimized with thinner dielectric layer and introduction of closely CTE matched polymer systems. Also CTE of the LCP can be engineered to the range 3 to 30 for better match with other dielectrics. Reworkability may not be an issue for low cost consumer products.

R L C passive components can be embedded using the build up technology proposed in Figure 2. For resistors, the authors have developed an electroless plating technology on BCB and LCP. The thin film resistors are alloys of NiP with temperature coefficient of resistance below 50 ppm/C. The sheet resistance is on the order of 100 to 400 ohms/sq with a thickness of 0.4 µm. For capacitors, the build up BCB can be filled in with low loss high dielectric constant particles and is expected to provide a capacitance density of 0.1 µF/cm^2 with reduced loss. Also electroless plating of BCB and LCP which will allow formation of interconnect copper lines, via filling with copper, and inductors with extremely high Q since the inherent loss of BCB is 0.0008 compared to conventional epoxy ~0.015.

Table 2. Advanced Materials with Ultrahigh Thermal Conductivities [5]

Reinforcement	Matrix	Inplane K W/m k	Through Thickness K, W/m k	Inplane CTE ppm/k	Specific gravity
	Cu	400	400	17	8.9
Diamond particles	SiC	600	600	1.8	3.3
Diamond particles	Cu	600-1200	600-1200	5.8	5.9
Carbon fiber	Cu	400 -420	200	0.5*	5.3*
	CVD diamond	1100-1800	1100-1800	1-2	3.5

*Properties can be tailoed

There are two viable paths for heat extraction: Ambient cooling and cooling with high thermal conductive plate attached to the backside of the chip. The first approach is conventional where ambient cooling can be leveraged with air jet or pumped liquid cooling. In the second approach, thin highly thermal conductive plate can be more efficient as heat sink (Table 2). For example, diamond-particle reinforced SiC composites are currently in use in IBM commercial servers [5]. Utilization of this material will

offer payoffs in reduced thermal stress and warpage, improved reliability and significant weight savings. Carbon fiber reinforced Copper metal matrix composites can also be engineered with isotropic fibers for more isotropic thermal properties.

Figure 3 shows another approach for the final multi-layer LCP construction utilizing the multi-layer lamination concept with laser cut cavity for embedding chips [6]. A 13-25-GHz GaAs bare die low noise amplifier is embedded inside a multilayer liquid crystal polymer (LCP) package made from seven layers of thin-film LCP. The active device is enclosed in a package consisting of several laminated CO_2 laser machined LCP superstrate layers. Measurements demonstrated that the LCP package and the 285C packaging process have minimal effects on the monolithic microwave integrated circuit radio frequency (RF) performance. These findings show that both active and passive devices can be integrated together in a homogeneous laminated multilayer LCP package. This active/passive compatibility demonstrates a unique capability of LCP to form compact, vertically integrated (3-D) RF system-on-a-package modules.

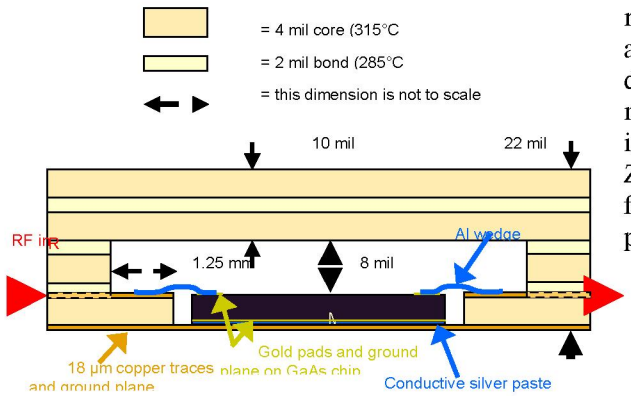


Figure 3. Embedded MMIC in multi-layer LCP

RFID tags on LCP

Printed electronic applications have enormous market potential. In a 2005 study, the British market research company, IdTechEx, estimated the market for organic electronics at 30 billion in 2015. Printed RFID tags will undoubtedly constitute a considerable part of this market. One of the great advantages of printed electronics is its ease of integration into products or packages. For example, they can be applied easily to flexible packaging materials by laminating or labeling, or by direct application. Thus, as a first step it becomes possible to apply labels with printed electronics, for example as an RFID tag, on to a product. Secondly, printed electronics can be integrated directly into the package and thus become 'intelligent' or 'smart' products. This means that packages/products can communicate through their RFID tag with a respective reader – hereby the vision of ubiquitous computing or the so-called 'internet of things' will be made possible. Conceivable applications for this technology include intelligent fridges, washing machines or better automation in production processes.

The exceptional characteristics of the RFID are exemplified in terms of antenna-IC matching and radiation efficiency on a flexible LCP substrate [7]. The 915 MHz passive tag is a 3" x 3" omnidirectional tag and yielded a read range of 31 feet compared to a 4" x 4" leading commercial design of 26 feet tested range in lab. This tag also possesses higher read power range (-7dBm to 30 dBm) than the leading commercial design (-5dBm to 30 dBm). The designed RFID antenna was fabricated on 50 micron thick Liquid Crystal Polymer (LCP) substrate and the read range of the proposed RFID tags was experimentally verified. A large format LCP sheet (300 mm x 300 mm) was used for antenna fabrication and the assembly of the IC was done using low temperature lead free solder alloys that are compatible with the heat distortion temperature of the LCP. In Fig. 4, the fabricated 18 um thick copper antenna on flexible, low-cost, and easily manufacturable LCP (ε_r =3.16, tanδ=0.002) with 50 µm thickness is shown. The antenna is also designed to accommodate space for other surface components such as a sensor module and a battery with minimum interference to the overall antenna performance. Maximum read range can be achieved when the dipole RFID antenna is half-wavelength resonant and has direction of current flow that adds up constructively. The tag size also plays a major role in determining the read range: The larger the tag, the larger is the energy capture area, therefore the longer the read range. One major difficulty in RFID tag design is designing the matching network since the chips come with either high or low input impedance phase angles. (i.e. Philips EPC 1.19 ASIC Zc=16-j350, NSC MM9647 Zc=73-j113). These three factors were taken into account to design optimum performing RFID tags.

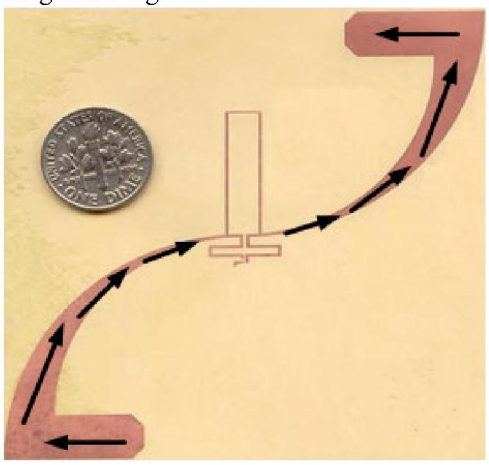


Figure 4. Fabricated RFID antenna and single dipole antenna direction of current flow

Paper-based substrates

The trend in RFID technology today is toward achieving more functionality ("wireless intelligence") at lower cost. In order to keep up with the demand, more complicated RFIDs must be built with progressively lower cost materials and processes that can be easily-integrated with other surface and/or embedded modules. Embedded paper electronics is a promising solution for this, and thus the goal for this study is to show the pathway toward achieving conductive interconnects for realization of complex circuitary on the cheapest synthetic material made by humankind. It is envisioned that integration of RFIDs

with paper-based pallets and containers would be one of the most critical requirements for item tracking and inventory control in hospitals and health care facilities. The flexibility and affordability of paper-based RFIDs opens possibilities for new applications such as anti-counterfeit protection and Electronic Article Surveillance. Paper-based substrate has great advantages (high reliability/life time and excellent high temperature stability) in terms of easy manufacturability compared to other plastic substrates such as PET. In addition to this, low thickness can be easily achieved with paper. For instance, adding a contactless smart label can significantly increase a document's overall thickness to encapsulate the IC. Plastic module needs 350 um thickness with a surface of 7 mm x 7 mm; meanwhile, paper module only uses 150 um thickness with a surface less than 11 mm^2 (equivalent to 2 sheets of 80g paper).

One of the objectives of this paper is to demonstrate the utilization of ultra-low-cost paper substrates for the realization of increased-functionality inexpensive RFID tags that can be integrated with batteries for further improvement of read/write range and with sensors for wireless sensing, tracking and monitoring. The conductors on the paper substrates are achieved by (i) direct write ink jet printing technology with tailored conductive ink and (ii) conventional copper etching upon lamination of metal foils on to the paper substrates. There are several issues in optimizing processes in either of the two approaches. For example, ink jet printing would require smooth surface finish, good adhesion, less smearing of the ink, fast curing profile, and ultimately copper-like conductivity of the printed ink and rapid prototyping for high volume manufacturing. On the other hand, metallization using copper will require bonding of copper onto paper surface, adhesion, compatibility with copper etch solutions and lithography, and moisture sealing. Both approaches have been successfully demonstrated for printing conductors on paper substrates which can be scaled to manufacturing. The copper metallization on paper substrates and dielectric characterization of paper substrates are realized for the first time ever. The final goal is to integrate RFIDs with sensors and thin film batteries for active tags with high read/write range wireless sensing in rugged industrial, warfare and automotive environments.

Paper is considered as one of the best organic substrates for RFID applications. First of all, paper is environmentally friendly and can undergo large reel to reel processing. In terms of mass production and increased demand, this makes paper the lowest cost material made. In addition, paper is compatible with circuit printing by direct write methodologies. This is one of the biggest advantages of paper since active tags require additional modules like sensors and batteries to be mounted on or embedded in. A fast process like inkjet printing can be used efficiently to print these modules on or in the paper substrate. Paper can also host nanoscale additives (i.e. fire retardant textiles) and can be made hydrophobic. Most importantly its dielectric constant ε_r (~3) is close to air's (5-6 % power reflection). Electromagnetic power can still penetrate easily even if the RFID is embedded in the substrate.

To achieve the ultimate goal of 3D paper-on-paper packaging with embedded passives, MEMS, RFIDs, sensors, thin film batteries, and discretes and ICs, several bottlenecks needs to be overcome since none of these processes have been optimized or even addressed. This paper addresses few critical steps toward achieving the end goal. A Roadmap for final goals is depicted below:

1. Development of moisture barrier coatings on papers
2. Characterization for dielectric constant and dielectric loss up to 40 GHz
3. Antenna design and optimization on characterized paper substrate
4. Antenna+IC+substrate integration and full RFID development
5. Design and system-level optimization by using the hybrid electromagnetics/mechanical optimizer
6. Performance Testing (Read range+ radiation pattern) and specific performance data checks
7. Materials development and optimization for thin film batteries
8. Optimize direct write technology for printing batteries
9. Prototype of thin film paper embedded batteries
10. Cost modeling (projected cost per RFID)

Selection of paper-material

Among critical needs for the selection of the *right* paper are the surface planarity, water-repelling, lamination for 3D construction, via-forming abilities, adhesion, and co-processability with low-cost manufacturing. For the trial runs, the selection was made by utilization of ink jet papers. The processes were developed for layer-to-layer lamination with inter-layer adhesion, copper foil lamination and etching, and with good quality of ink-jet printing with conductive inks. Work is in progress with hydrophobic papers and selection of proper hydrophobic coating on conventional papers.

Measurement of dielectric constant and dielectric loss

This is the critical step that must be qualified for utilization of new material for a wide range of frequency domain application. The precise methods are microstrip ring resonators, parallel plate resonators, and cavity resonators [8]. The cavity resonator method is used in this paper to determine the dielectric constant by measuring the shift in the resonant mode [8,9]. Thus the measured dielectric constant is found to be 1.6 at 34 GHz fixed frequency calculated from the shift in TE_{011} shown in Figure 5. A diagram of the cavity resonator with different frequencies of operations is shown in Figure 6. These are preliminary results and current being verified by ring resonator method where dielectric constant can be extracted at a continuous frequency band.

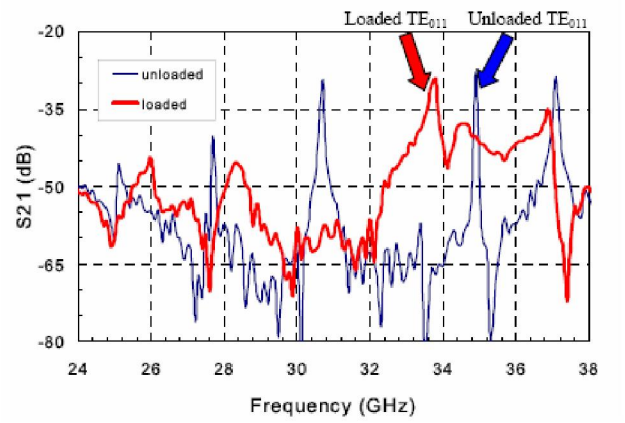


Figure 5. Measured mode shifting of the unloaded/loaded split cylinder cavity.

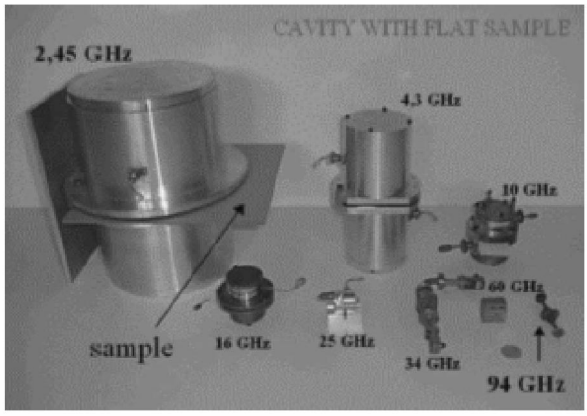


Figure 6. Cavity resonators with different measurement frequencies [8]

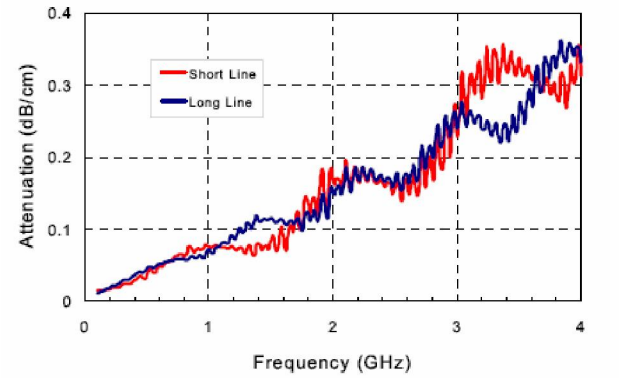


Figure 7. Measured dielectric loss of a hydrophobic paper using transmission line calibration.

For calculation of total dielectric loss, a TL method was used. In this method the dielectric loss (a_d) of a microstrip line can be extracted

$$\tan\delta = \frac{a_d \lambda_o \varepsilon_e^{1/2} (\varepsilon_r - 1)}{\pi \varepsilon_r (\varepsilon_e - 1)} \quad \ldots\ldots (1)$$

using equation 1, where λ_o is the free space wavelength, ε_e is the effective dielectric constant, ε_r is the relative dielectric constant [8]. Measurement (Figure 7) was recorded using Agilent VNA in the range 0.1 GHz to 4 GHz. The dielectric loss (tan δ) of the substrate was found 0.077 at 900 MHz and 0.082 at 2.4 GHz. The attenuation increases as expected with the increase in frequency.

Printing conductors by ink-jet and copper etching

Two methods were qualified for printing conductors. The first being an ink-jet printing similar to direct write method. A low-cost Dimatix printer system is used with especially formulated conductive silver ink from Cabot Corporation. Figure 8 shows a fabricated RFID tag on an ink-jet paper surface. High throughput would be required for commercialization with ink jet type direct printing method. Figure 9 shows development of new generation Dimatix printers that can handle high throughput [10]. The ink jet printing technology has already been adopted for direct writing passives components such as capacitors, resistors, and inductors by numerous companies.

The second method is conventional lamination and copper etching chemistries. This is much more operator intensive but can be easily adopted in a PCB fabrication house and therefore more attractive toward large volume manufacturing at lower cost. This method has also been optimized with six layers of laminated paper substrates with top and bottom layers of laminated 18 micron copper followed by etching of copper to form 50 and 100 microns lines and spaces. A ring resonator with calibration lines was made using conventional copper etching for dielectric characterization of paper substrates.

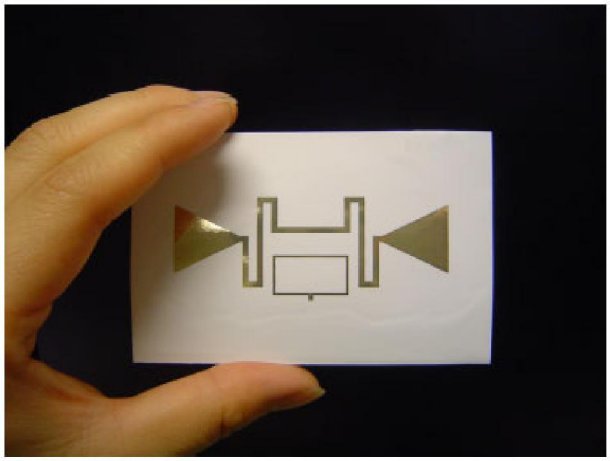


Figure 8. Ink-jet printed RFID tag on paper using Dimatix printing system.

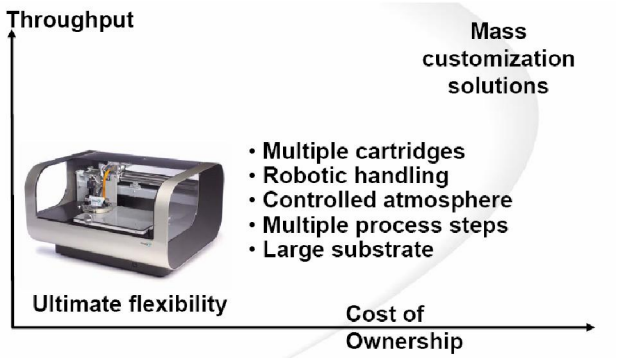


Figure 9. Dimatix printers from Research and development toward commercialization [10].

Paper-on-paper – 3D packaging with embedded IC

A multi-layer core has been fabricated using paper-on-paper, the thickness achieved is 1.2 mm using six

layers of ink-jet printable copper. The current work is focused in printing passives structures (R, L, and C) and then laminate to form a multi-layer structure with cut out cavity for embedding active chips similar to what has been accomplished for the LCP substrate shown in Figure 3.

Embedded thin-film batteries

Embedding thin film batteries will have unparallel advantages from cost, size, and performance advantages. The size of the batteries is becoming bottlenecks for miniaturization of hand-held products. With embedded thin film batteries where the conductors will be printable and the electrolytes will be the polymer gels that can be incorporated in multilayer paper constructions. The embedded self-charging batteries will also serve as the powersource for active antennas. This is still in the conceptual stage.

A block diagram of the active RFID tag with embedded thin film batteries and sensors currently being built is shown in Figure 10.

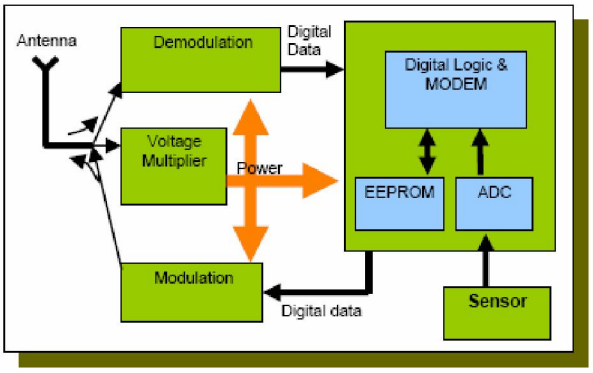


Figure 10. Block diagram of the RFID tag

Conclusions

Today's packaging is dominated by SMT components for both actives and passives. However, due tremendous restriction in available real estate on the surface and the drive for thin packages, embedding passives and actives has been receiving interest both from materials and manufacturing standpoint. The challenges and the state-of-the-art in embedded RLC, discretes, and actives in thick and thin packages have been summarized in this paper. In a cost driven market, the ultimate success will depend on the choices of lowest cost material and manufacturing processes. To address the cost issues, the RFID/Sensor group at Georgia Electronic Design Center is looking into realization of embedded components, actives, sensors, RFIDs for wireless sensing that can be adopted in the application horizon covering supermarkets to bio-hazards, security, medical as well as defense application. This paper elutes the basic steps toward application of paper-based substrates for functional circuitary. The first step is in authors view is to characterize electrical properties such as dielectric constant as a function of frequency up to at least 10 GHz which has been achieved for the first time for the paper substrates using cavity resonator method. The second step is forming conductive paths on the paper surface. Two approaches have been taken – conventional lamination/etching of copper as well as ink-jet printing – both have been optimized for the first time. 3D paper-on-paper packages similar to LTCC green sheets are under constructions. Hydrophobic coatings are being investigated for the protection of moisture penetration that could disturb the stability of electrical performances. The outcome in the near future would be a flexible 3D embedded package with embedded actives and passives and thin film battery in paper-substrates which is expected to be the ***lowest*** cost scenario for the first time ever.

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