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Flip-Chip vs. Wirebond

There's no clear winner yet in the microwave and millimeter-wave arenas

By Daniela Staiculescu, Kyutae Lim, Albert Sutono, Hongwei Liang, Manos Tentzeris and Joy Laskar

Tougher competition in existing wireless communication markets and emerging wireless applications that utilize a higher frequency spectrum are pushing hardware vendors to make more competitive products (such as the front-ends and the passive and active components). In the last few years, the need for high integration levels for RF and microwave applications have made the choice of interconnection solutions a very important issue, especially since the quality of these interconnects has a major impact on the performance and cost of the entire system. The need for better electrical performance—along with the cost reduction necessary for achieving the large growing potential of the wireless market—make vertical interconnections very promising.

In recent years, both level-1 (chip-to-package) and level-2 (package-to-board) vertical interconnects have been considered. This article will summarize the advantages and the drawbacks of flip-chip vs. the widely used wirebond for microwave and millimeter-wave (mm-wave) applications, and how these affect the job of designers and engineers. As an alternative solution, ball grid array (BGA) packaging also will be addressed.

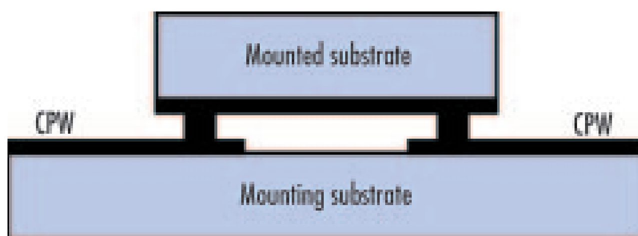

Figure 1 - Flip-chip schematic

Configurations for comparison

Flip-chip is a solder ball array for level-1 of assembly (chip-to-package). The example illustrated in **Figure 1** is a side view of a coplanar waveguide (CPW) to CPW flip-chip interconnection including three bumps—two for ground and one for signal. **Figure 2** shows the photograph of a flip-chip ball before and after the bumping process.

The wirebond, also a level-1 interconnection solution, is generally used in microstrip configurations. **Figure 3** illustrates a sideview of a wirebond test vehicle.

General aspects

Although new packaging and interconnection technologies have been introduced, wirebonding is still dominant in RF/wireless products since it has strong benefits in cost and reliability. However, the stringent specifications of emerging communication systems and use of higher frequency band cause the engineer to be concerned about the drawbacks of wirebonding—e.g., parasitic effect and losses. Wirebond used as an interconnection in a microwave and mm-wave module exhibits a high characteristic impedance due to the high inductance of thin wire diameter and a small capacitance due to the small dielectric constant of air gap between wire and ground plane. In addition, radiation loss resulting from wire discontinuity becomes significant, particularly in the mm-wave frequency range.

Vertical interconnection solutions have gained a significant interest because they provide features that can eliminate the problems associated with wirebonding: poor repeatability of the manufacturing process and a drastic increase of the losses associated with increased frequency. Along with showing better electrical performance, flip-

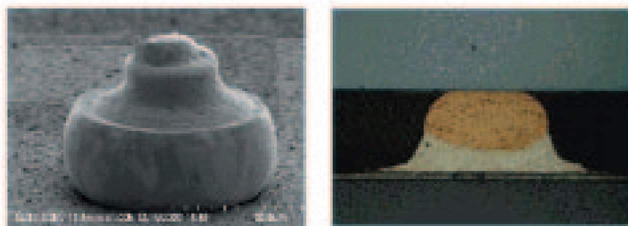

Figure 2 *- Picture of flip-chip bump. The flip chip ball before (left) and after (right)*

chip technology allows several chips to be mounted together on the motherboard to increase density, improve system performance and reduce cost (see **Reference [1]**). This packaging technique also allows combinations of active and passive devices, silicon (Si) and gallium arsenide (GaAs), and probably analog and digital circuits on the same motherboard. Furthermore, the compatibility with automatic manufacturing improves the reliability and reduces assembly cost. For microwave circuit applications, low cost, high density and short transition interconnects are considered to be the main advantages of the flip-chip technique.

In addition to these benefits, since the die in flip-chip is flipped upside down, all the chip area is available for interconnect, eliminating the wirebond restriction of having all the I/Os along the chip perimeter. This, along with the short electrical path which eliminates coupling issues, allows true chip-scale packaging and therefore increased integration levels.

Another important issue is the transmission line choice. The two most common choices for the transmission line to be used in a flipped, monolithic microwave-integrated circuit (MMIC) are microstrip and CPW. Coplanar MMICs are more suited to flip-chip technology due to the immediate availability of all the grounds on one surface. In addition, coplanar circuitry requires no backside processing, eliminates the need for ground vias and allows the use of a thicker, more physically robust chip. Better matching with coplanar transmission lines is possible due to the ground-signal-ground configuration. On the other hand, microstrip design tools are more popular and MMIC manufacturers prefer to make full use of their capabilities.

However, thermal performance of flip-chip packages is poor compared to wirebond. Heatsinking is more efficient when the chip is fully sitting on the vertical stack-up rather than having no other contact with it than the interconnecting bumps. The coplanar design of the PCB eliminates the need for the vias, and shunt elements can be easily removed or added if tuning is necessary.

From a mechanical reliability standpoint, flip-chip technology still needs to be improved. An underfill technology—to fill the gap between the chip die and board with a dielectric material—has been introduced to improve the heat dissipation and the mechanical stability and to compensate CTE mismatch. However, it is difficult to apply underfill technology for RF modules, since the additional dielectric loss generated from the underfill material will reduce the

Figure 3 *- Wirebond schematic*

system efficiency. Moreover, characteristic impedance of the transmission lines on an MMIC chip will be significantly changed due to the higher dielectric constant of the material. To avoid this problem, all of the MMIC circuits should be designed to compensate the expected impedance change.

Comparison of electrical performance

A comparative analysis using microwave measurements of similar wirebond and flip-chip test structures is presented in **Reference [2]**. Two identical CPW transmission lines on GaAs substrate have been attached to a ceramic motherboard using both wirebond and flip-chip. The wirebond assembly has been realized with the shortest loops possible. The measurement of the insertion loss to 75 GHz shows a considerable difference between the two test structures, with almost 1dB at 75 GHz. The better electrical performance of the flip-chip compared to wirebond is caused by the minimized parasitic

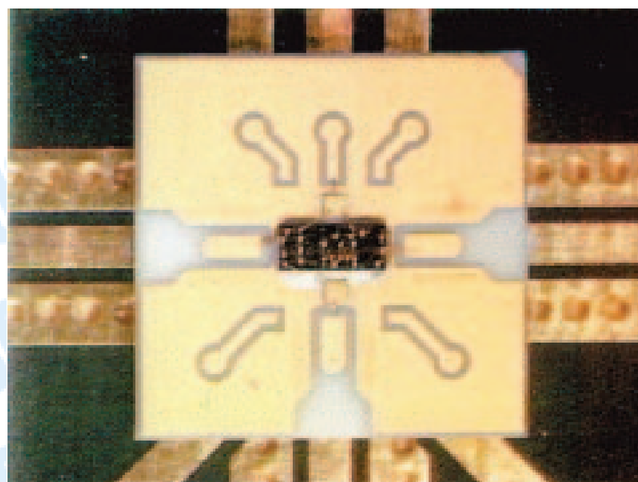

Figure 4 *- Wideband LNA with BGA package*

effects associated with the shorter chip-substrate transition. **Reference [3]** shows another comparison between wirebond and flip-chip.

Measurement and simulation of the wirebond interconnection insertion loss for three different wire lengths: 50 µm, 410 µm and 700 µm showed worse performance than a similar structure using flip-chip with a bump height as high as 200 µm. It is worth mentioning that the performance of the interconnections are strongly dependent on the material of the base substrate, type of conductor, the length and number of interconnections and the location of nearby ground, as well as the maturity of the process. This implies that suggesting an absolute figure of frequency of operation in any technology would be difficult.

For the package-to-board level of packaging, the bump interconnection method is BGA. Since the early 1990s, the BGA package has been widely used in electronic packages, including high-speed CPU/microprocessors and the chip-to-board interconnections for Gbps network boards. Basically, the advantages of using BGA technology refer to the same issues as flip-chip. Although flip-chip has better frequency performances and less loss than BGA, BGA has advantages in reliability and cost perspectives over flip-chip. In microwave and mm-wave applications, it has been successfully shown that the BGA package can support up to 40 GHz with the insertion loss of less than -1 dB and –10 dB return loss. **Figure 4** shows the BGA-packaged wide band LNA for 20-40 GHz. The inser-

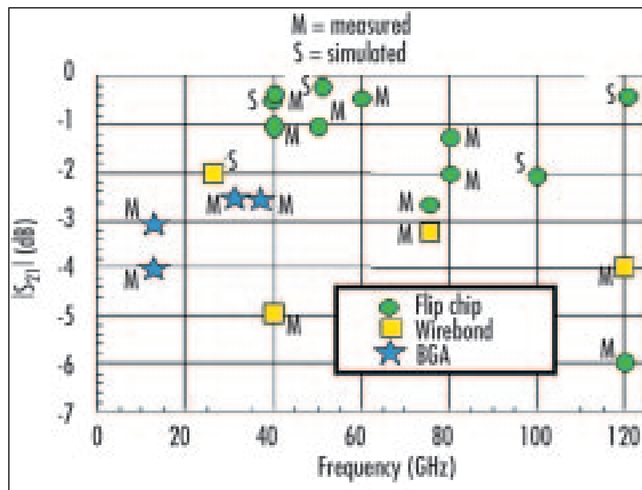

***Figure 5** - Summary of |S21| results for flip-chip, wirebond and BGA*

tion loss degradation due to the package is negligible (see **Reference [4]**).

Figure 5 presents a review of the published insertion loss results for wirebond, flip-chip and ball grid array interconnections (see **References [5] through [16]**). The test structures used in these analyses are not identical and the individual characteristics are reflected in the S-parameters. However, it is observed that flip-chip shows evidence of lower insertion loss over the entire frequency range than wirebond. On the other hand, BGA performance is poor compared with flip-chip, as a result of the larger dimensions and the use of lossy substrates for the motherboard. Similar results have been reported for return loss.

Conclusion

One of the key issues in the RF area is interconnection technology, which enables low cost and better performance of RF systems. A review of the existing technologies showed that many of the large companies conducting research and development in the field of packaging interconnects develop a growing interest in flip-chip vs. the widely used wirebond. High density and low cost are among the main advantages of flip-chip technology, along with the flexibility given by the coplanar design. Comparisons of electrical characteristics of flip-chip and conventional wirebond packages showed the superior performance of flip-chip. Still, thermal performance is poorer for flip-chip due to the limited heatsinking capability of the bumped die.

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