Crosstalk Between Finite Ground Coplanar Waveguides Over Polyimide Layers for 3-D MMICs on Si Substrates

John Papapolymerou, *Senior Member, IEEE*, George E. Ponchak, *Senior Member, IEEE*, Edan Dalton, Andrew Bacon, and Manos M. Tentzeris, *Senior Member, IEEE*

***Abstract*—Finite-ground coplanar (FGC) waveguide lines on top of polyimide layers are frequently used to construct three-dimensional Si–SiGe monolithic microwave/millimeter-wave integrated circuits on silicon substrates. Requirements for high-density, low-cost, and compact RF front ends on silicon can lead, however, to high crosstalk between FGC lines and overall circuit performance degradation. This paper presents theoretical and experimental results and associated design guidelines for FGC line coupling on both high- and low-resistivity silicon wafers with a polyimide overlay. It is shown that a gap as small as 6 μm between two adjacent FGC lines can reduce crosstalk by at least 10 dB, that the nature of the coupling mechanism is not the same as with microstrip lines on polyimide layers, and that the coupling is not dependent on the Si resistivity. With careful layout design, isolation values of better than -30 dB can be achieved up to very high frequencies (50 GHz).**

***Index Terms*—Coplanar waveguide (CPW), coupling, crosstalk, finite difference time domain (FDTD), finite ground coplanar (FGC) waveguide, monolithic microwave integrated circuit (MMIC), polyimide.**

I. Introduction

WITH THE ever-increasing demand to produce high-density, low-cost, and compact RF front ends for high data rate, wireless communication systems, and high-resolution radars, there has been a large amount of research, both in industry and in academia, to develop high-quality microwave circuits and modules on silicon substrates. The choice of the silicon substrate is primarily driven by the low processing cost and the capability to monolithically integrate SiGe devices that have exhibited cutoff frequencies up to 350 GHz [1]. The latter advancement has paved the way for the realization of a fully monolithic microwave system-on-a-chip (SOC) that can operate up to millimeter-wave frequencies in contrast to a system-on-a-package (SOP) where the active devices are fabricated separately from the rest of the circuitry and integrated at the end. The development, however, of high-frequency active devices is not the only requirement for the realization of such a complicated SOC. The integration of a large number of passive components (e.g., transmission lines, inductors, capacitors, filters) with small loss and minimal crosstalk is as important as the advancement in the diode and transistor technology. Since waveguide components that are known for their high-quality factors cannot be used in compact SOC architectures, novel concepts are needed to address the passive components associated issues. Of recent particular importance is the crosstalk or isolation between the various circuits, as the degree of integration has increased dramatically to minimize the development cost.

The first efforts that addressed the quality-factor issues of passive components associated with silicon substrates, which typically have higher loss than other traditional microwave substrates (e.g., GaAs or alumina), focused on using high-resistivity Si wafers. A variety of passive structures have been developed on silicon with resistivities ranging anywhere from 1000 $\Omega \cdot$ cm to 20 k$\Omega \cdot$ cm [2]–[7]. In most cases, the performance of these elements rivaled the performance on GaAs or on insulating materials. However, the associated development cost is higher than using low-resistivity silicon, especially when active devices need to be integrated with the use of a CMOS processing technology. For these reasons, researchers also focused on developing passive elements on CMOS and BiCMOS type ($\rho = 0.01$–$20\ \Omega \cdot$ cm) substrates with a goal to minimize the loss and interaction. More specifically, efforts focused mostly on using a variety of relatively thin (5–20 μm) dielectric layers (e.g. polyimide, benzocyclobutene (BCB), oxide) with a goal to minimize the electromagnetic-field interaction of the passive structures with the lossy Si substrate [8]–[12]. Some efforts also focused on removing (micromachining) part of the Si substrate [13], [14] in order to totally remove the deleterious substrate effects.

Two types of transmission lines for CMOS-type silicon substrates have been developed thus far, which are: 1) the thin film microstrip line (TFMS) and 2) the finite ground coplanar (FGC) line with an insulating interface layer. The TFMS is comprised of a metal layer deposited on top of the lossy silicon and the actual line deposited on top of the dielectric layers. In this way, the dielectric layers act as the substrate and the metal ground plane provides perfect shielding of the electromagnetic fields

Manuscript received September 15, 2003; revised December 18, 2003. This work was supported by the National Science Foundation (NSF) under CAREER Award 9984761, by the NSF under Small Grant for Exploratory Research Award 0196376, by the Georgia Electronics Design Center, and by the Georgia Tech Packaging Research Center.

J. Papapolymerou, E. Dalton, and M. M. Tentzeris are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA.

G. E. Ponchak is with the Glenn Research Center, National Aeronautics and Space Administration, Cleveland, OH 44135 USA.

A. Bacon was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA. He is now with Northrop Grumman, Baltimore, MD 21090 USA.

Digital Object Identifier 10.1109/TMTT.2004.825714

0018-9480/04$20.00 © 2004 IEEE

from the Si substrate. TFMS solved the problem of high loss and compact circuits. Coupling between two parallel TFMS lines embedded in thick polyimide layers was also studied recently [15] and showed that acceptable levels (>40 dB) of isolation can be achieved if shielding structures are used. The FGC line was developed to overcome some of the problems associated with microstrip lines, such as difficulty of integrating both series and shunt elements, via-holes, backside processing, and limited impedance range for the dielectric overlay on top of the lossy silicon. The FGC line consists of one signal conductor, two slots, and two ground planes of finite width (typically 2–4 times the signal width) on top of the thin dielectric layer. Two versions of the line exist: the one with conductor backing (metal on top of the silicon) and the one without backing. The former is notorious for exciting higher order modes that can increase dispersion, as well as cross-coupling. The latter does not suffer from this problem and, indeed, the cutoff frequency of the higher order modes can be controlled by the ground-plane width. In addition, FGC line passive circuitry can be processed in one step since all metals are on the same layer; the line can support an almost pure TEM mode of propagation up to 120 GHz, and is well suited for flip-chip interconnects. Lastly, a wider impedance range can typically be achieved than with the TFMS line. To use FGC lines on silicon wafers with resistivities used for CMOS circuits, a thin dielectric layer between the FGC line and silicon is required to minimize electromagnetic-field interaction with the Si substrate. This has enabled measured attenuation levels of around 3 dB/cm at 25 GHz to be reported [16]. Care should be exercised, however, when designing FGC lines on CMOS-type silicon substrates with dielectric overlays, as considerable loss can be attained [14], [16]. Coupling is very small between FGC lines on high-resistivity silicon (HRS) substrate (no dielectric overlay) [17]. In [17], it was observed that FGC lines on HRS substrates have approximately 8 dB lower coupling than coupled coplanar lines and that their forward and backward coupling characteristics do not resemble those of other transmission lines such as microstrips. An FGC line fabricated on an insulator over a semiconductor can support, in general, three modes of propagation (a coplanar-waveguide (CPW) mode, a dielectric quasi-TEM mode, and a slow-wave mode). In addition, surface waves may exist on the substrate that may further degrade the FGC circuit isolation. However, since the FGC line has less field overlap with the surface-wave modes than the microstrip line, it interacts weakly with them [18], theoretically providing better isolation than the microstrip lines.

This paper investigates the coupling effects of FGC lines on silicon substrates with a thin dielectric overlay. Preliminary results that only include the measured coupling of FGC lines on HRS with a polyimide overlay were reported in [19]. This paper presents for the first time results for FGC lines on CMOS-type substrates with a polyimide overlay and, therefore, provides a more complete understanding of the coupling effects that may exist in such structures. The parasitic crosstalk between FGC lines on low-resistivity silicon substrate is analyzed to determine the effect that the distance between adjacent finite grounds has on the coupling of their associated lines. In addition, a physical analysis of the various modes that exist on the coupled FGC lines is presented for the first time to better understand the measured results. Since FGC lines are wider than microstrip lines, space requirements could be a drawback for this type of lines in RF packages and interconnects. A minimum distance between adjacent FGC lines to prevent significant crosstalk is important to conserve area. Simulations using the finite-difference time-domain (FDTD) technique were employed to identify the spacing requirements for minimum crosstalk, and measurements were taken to verify those results.

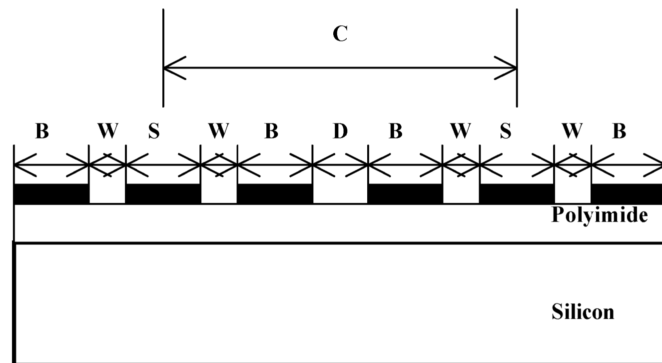

Fig. 1. Cross-sectional view of adjacent FGC lines.

II. Circuit Description

The FGC structures were designed over a multilayered substrate comprised of a layer of polyimide over silicon. Fig. 1 illustrates a cross-sectional view of two adjacent FGC lines that lie on top of the same polyimide layer. The distance between the edges of their finite grounds is D, the distance between the centers of the two FGC lines is C, and the widths of the center (signal) conductor, slot, and ground-plane conductor are S, W, and B, respectively.

All experiments were performed for adjacent FGC lines of the same geometry and impedance. The FGC structures that were analyzed had dimensions of $S = 42$ μm, $W = 24$ μm, and $S = 20$ μm, $W = 10$ μm, with values of B ranging from 20 to 84 μm. Five cases for the value of D were studied, i.e., $D = 0$ (common ground), $D = 6$ μm, $D = 12$ μm, $D = 18$ μm, and $D = 30$ μm. The design for the FGC lines was aided with methods found in [20]. Although the presented procedure for finding an effective dielectric constant for the multilayer substrate was derived for a CPW structure with infinitely long ground planes, it was very useful in determining approximate impedance and guided wavelengths, and can be adapted for FGC lines. It begins by transforming the individual dielectric layers of finite thickness into dielectric layers of semi-infinite thickness by using a mapping transformation that is independent of the dielectric constant for the materials and is based strictly on geometry of the CPW lines. From this data, filling factors for the individual layers are determined by comparing the capacitance of the substrate layer using the original dielectric value with the capacitance of the same substrate layer replacing the dielectric with air. The filling factors determine how much each layer contributes to the effective dielectric constant of the overall structure. Once the effective dielectric constant is found, the characteristic impedance of the line can also be determined.

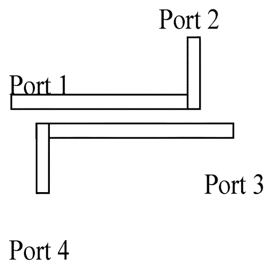

Fig. 2. Schematic of coupled-line structures used for coupling characterization.

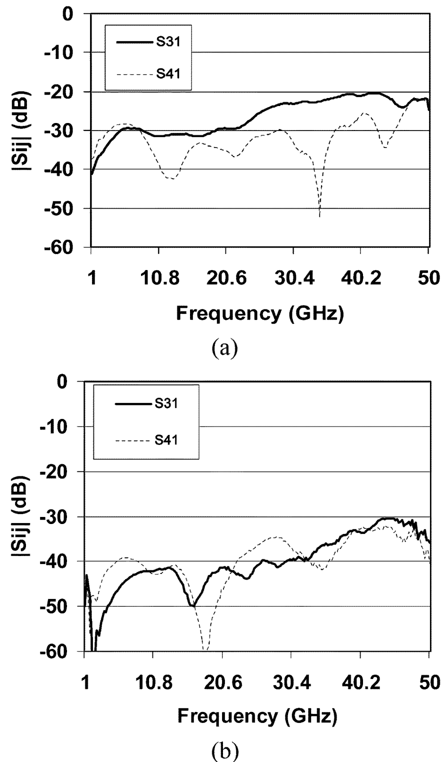

Fig. 3. Measured coupling parameters for FGC lines fabricated on low-resistivity Si with $S = 42$ μm, $W = 24$ μm, and $B = 84$ μm. (a) $D = 0$. (b) $D = 6$ μm.

Results from this analysis, which is based on the conformal-mapping techniques presented in [20], were used as the starting point for the design of the desired FGC lines. The FGC line geometry was then analyzed and optimized with the help of a full-wave simulation tool Sonnet based on the method of moments. Sonnet simulations take into account the substrate parameters (thickness and loss), as well as the metallization parameters (thickness and conductivity). For the $S = 42$ μm, $W = 24$ μm FGC line, the simulations yielded an $\varepsilon_{\rm eff} = 2.8$ and a $Z_0 = 75$ Ω, while for the $S = 20$ μm, $W = 10$ μm, they yielded an $\varepsilon_{\rm eff} = 2.3$ and $Z_0 = 81$ Ω at a frequency of 15 GHz for a low-resistivity silicon substrate.

III. Circuit Fabrication

For the fabrication of coupled FGC lines and their characterization, the thickness of the polyimide layer utilized as the insulation layer was 20 μm of Dupont PI-1111 with a dielectric constant of 2.8. A single layer of this material was spun onto a

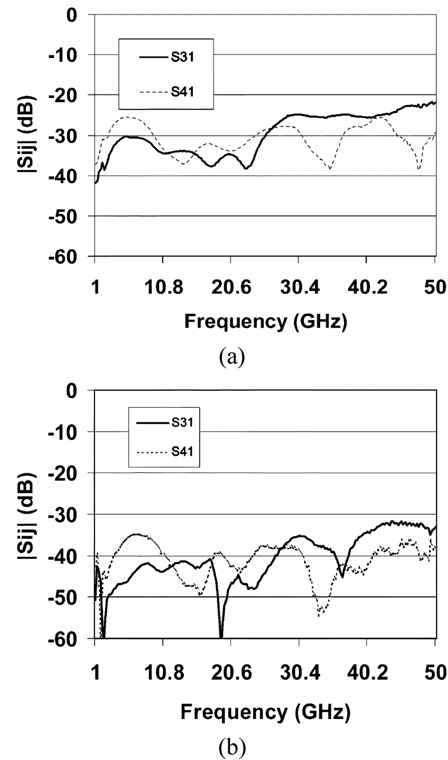

Fig. 4. Measured coupling parameters for FGC lines fabricated on low-resistivity Si with $S = 20$ μm, $W = 10$ μm, and $B = 20$ μm. (a) $D = 0$. (b) $D = 6$ μm.

500-μm silicon wafer. The silicon wafers had both high (greater than 1000 $\Omega \cdot$ cm) and low resistivities (less than 5 $\Omega \cdot$ cm). After curing the polyimide, 200 Å of titanium and 1.5 μm of Au were evaporated onto the polyimide coated wafer and a pattern was defined with a liftoff process. Fig. 2 illustrates the layout of the fabricated lines, which have a coupling length of 7500 μm. Ports 2 and 4 are on right-angle bends to prevent coupling of the ports during their excitation and facilitate the RF probe positioning.

In the fabricated circuits, air bridges were placed every 1500 μm along each FGC line to suppress any slotline modes from forming. The air-bridge width was 40 μm and the length was equal to $S+2W$. To construct the air bridges, a single 3-μm layer of PI-2611 polyimide with relative permittivity equal to 3.12 was spun onto the wafer and cured. Ni was evaporated onto the polyimide to serve as a mask for the O_2/CF_4 reactive ion etching (RIE), which was used to etch via-holes through the PI-2611 to the ground planes of the FGC lines. The via-hole size was 40-μm square and they were located 3 μm away from the edges of the FGC line slots. After the via-holes were etched and the Ni mask removed, the bridges were defined by a liftoff process consisting of 200 Å of titanium and 1.5 μm of gold to connect the plated vias. Via-holes were also created in the RF probing areas.

IV. Measured Results

The measured cross-coupling results for the two different FGC line geometries ($S = 42$ μm, $W = 24$ μm, $B = 84$ μm and $S = 20$ μm, $W = 10$ μm, $B = 20$ μm) and two different

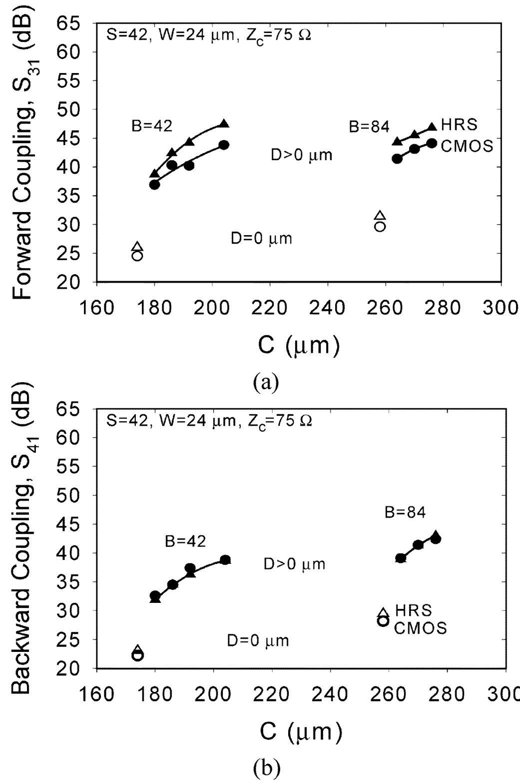

Fig. 5. Summarized: (a) forward coupling and (b) backward coupling for FGC lines with $S = 42$ μm and $W = 24$ μm fabricated on high- and low-resistivity Si. Coupling shown is the maximum coupling measured for $f < 10$ GHz. High-resistivity data are from [19]. $D > 0$ corresponds to $D = 6, 12, 18,$ and 30 μm. The $\triangle$ are for the FOC lines on HRS, the ○ are for the FGC lines on CMOS Si.

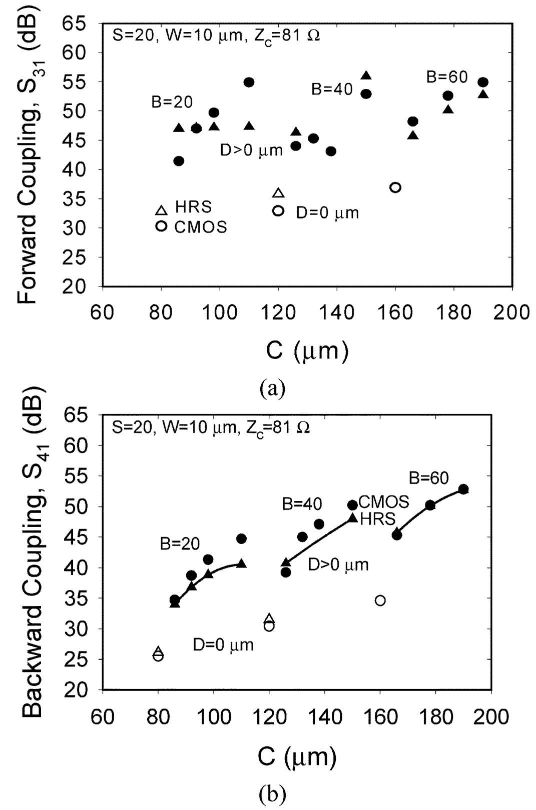

Fig. 6. Summarized: (a) forward coupling and (b) backward coupling for FGC lines with $S = 20$ μm and $W = 10$ μm fabricated on high- and low-resistivity Si. Coupling shown is the maximum coupling measured for $f < 10$ GHz. $D > 0$ corresponds to $D = 6, 12, 18,$ and 30 μm. The $\triangle$ is for the FGC lines on HRS and the ○ is for the FGC lines on CMOS Si.

values of separation distance D for low-resistivity silicon are shown in Figs. 3 and 4. For the high-resistivity case, the results can be found in [19]. The insertion loss (S_{21}) shows the attenuation of a signal through the 7500-μm-long FGC line, but since the primary emphasis of this paper is the isolation and cross-coupling, S_{21} is not plotted. First, the backward coupling defined as $-20 \log |S_{41}|$ and the forward coupling defined as $-20 \log |S_{31}|$ for the FGC line with $S = 42$ μm, $W = 24$ μm, $B = 84$ μm, and $D = 0$ have the typical characteristics of monotonically increasing forward coupling with frequency and backward coupling that is periodic with frequency (several dips), as shown in Fig. 3(a). The forward coupling reaches a maximum value of -20 dB around 40 GHz. The results are similar for the same line geometry on HRS [19]. When the separation distance D is increased to 6 μm, the forward and backward couplings are reduced and increase with frequency, but dips are observed in the forward coupling, as shown in Fig. 3(b). Similar dips were also observed in the high-resistivity case [19] when $D = 6$ μm. The maximum value of coupling is around -30 dB at approximately 45 GHz and this is also in agreement with the high-ρ case. This behavior (nonmonotonic increase) observed in the forward coupling for both high- and low-ρ silicon wafers is not similar to results presented in literature for coupled transmission lines such as microstrips [15], [21]. In this case, it is believed that the forward and backward coupling when $D > 0$ is due to indirect coupling, as described by Schelkunoff and Odarenko [22]. This indirect coupling is a result of a parasitic mode due to the ground planes of each FGC line that create a third transmission line. To further verify this, a full-wave electromagnetic analysis is performed in Section V. For the second FGC line geometry ($S = 20$ μm, $W = 10$ μm, $B = 20$ μm), measured results presented in Fig. 4 show a similar behavior to that of the first FGC line. For a small separation of $D = 6$ μm, the forward coupling increases in a nonmonotonic fashion and results in coupling values less than -30 dB up to 50 GHz. It should be noted here that this transmission line has a slightly higher impedance. For the $D = 0$ case, both forward and backward coupling are below -20 dB.

Figs. 5 and 6 summarize this reduction in coupling by plotting the maximum coupling measured for $f < 10$ GHz for each of the structures characterized. For comparative purposes, the data of exactly the same line geometries on HRS ($\rho = 2500$ Ωcm) are also plotted. It is seen that there is a large reduction in coupling when $D > 0$ ($D = 6, 12, 18,$ and 30 μm), even when D is as small as 6 μm, which implies that the nature of the coupling changes when $D > 0$. Also, it is seen that for the electrically short coupled-line sections shown in Figs. 5 and 6, the backward coupling is approximately 3–5 dB higher than the forward coupling. For the $S = 42$ μm, $W = 24$ μm coupled lines, Fig. 5 shows that backward coupling is practically identical for the high- and low-resistivity (CMOS) cases, while for the forward coupling, the CMOS case is approximately 1–2 dB higher

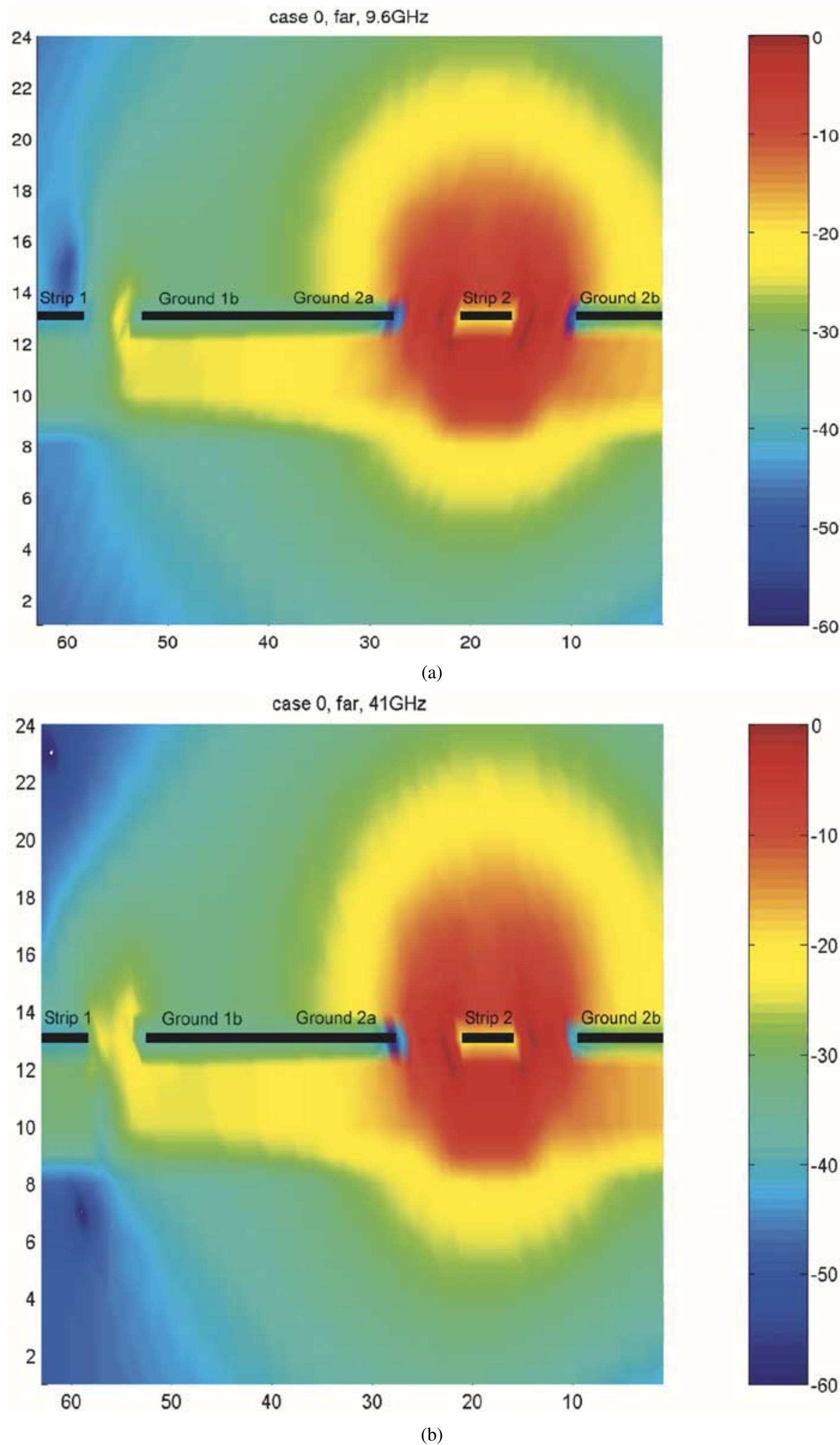

Fig. 7. Electric-field plots for the $S = 42$ μm, $W = 24$ μm, and $B = 84$ μm FGC line where $D = 0$ μm. Field plots are taken at various frequencies. (a) 9.6 GHz. (b) 41 GHz.

when $D > 0$ depending on the ground-plane width. Fig. 5 also reveals that for larger ground-plane widths and, thus, larger center-to-center distance C, but for same S and W, both forward and backward coupling are 2–5 dB lower for both cases of silicon resistivity. For the $S = 20$ μm and $W = 10$ μm coupled FGC lines, Fig. 6 shows that there are very small differences in the backward coupling between the high- and low-resistivity cases for different values of B and D. The highest difference

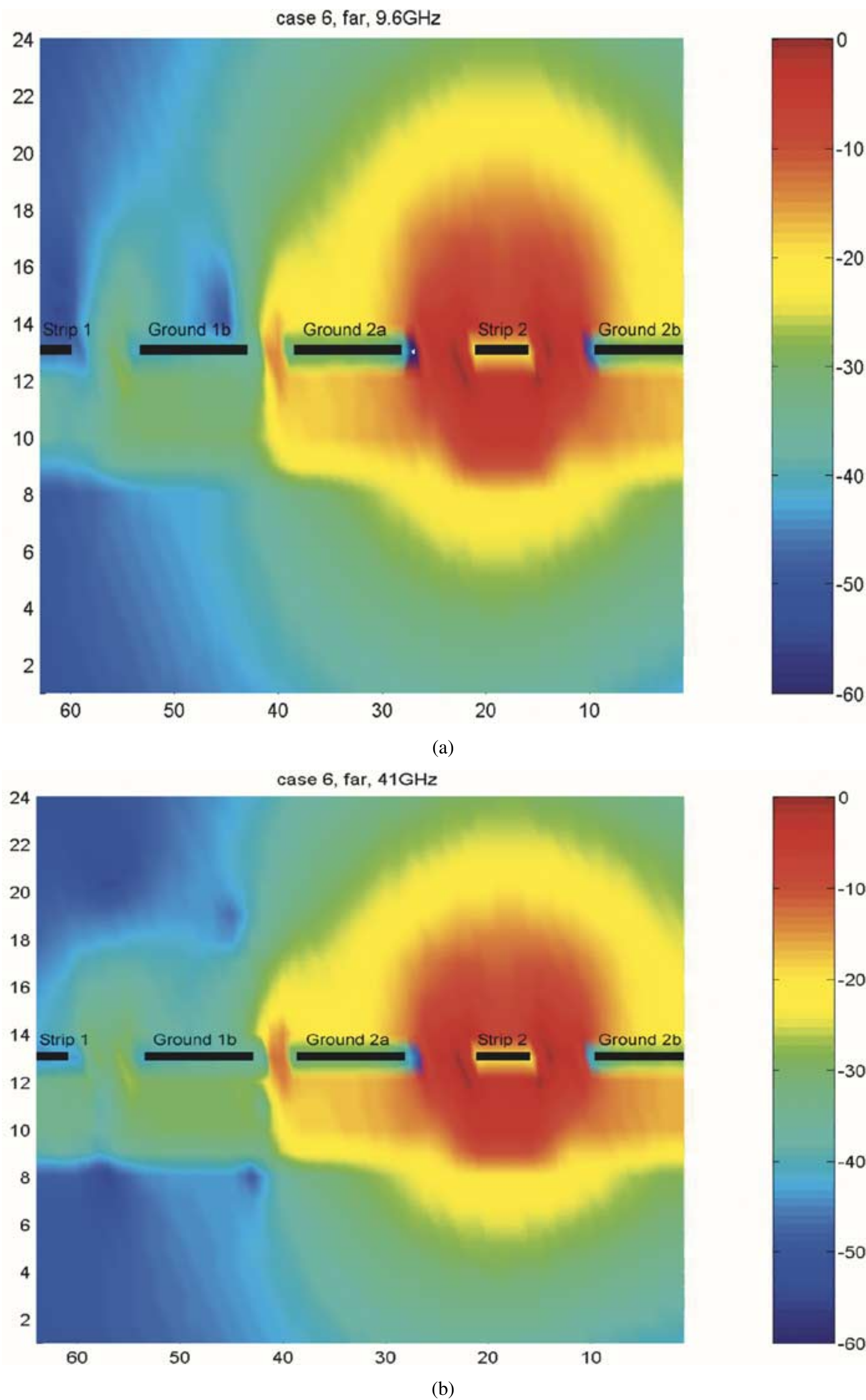

Fig. 8. Electric-field plots for the $S = 42$ μm, $W = 24$ μm, and $B = 84$ μm FGC line where $D = 6$ μm. Field plots are taken at various frequencies. (a) 9.6 GHz. (b) 41 GHz.

($\sim$4 dB) was measured for the $B = 20$ μm, $C = 110$ μm, and $D > 0$ cases. For the forward coupling case of this line, when $D = 0$, the CMOS results indicate a 1–2 dB increase with respect to the high-ρ results, as was the case of the first line geometry.

The measured difference in coupling of FGC lines on high- and low-resistivity silicon wafers with a polyimide interface layer is very small, less than 2 dB, and there does not appear to be a consistent trend in the difference. Considering that this small difference concerns S-parameters with values from -25 to -45 dB, it appears that this difference is due to measurement and data analysis errors and that the coupling does not depend significantly on the substrate resistivity. Furthermore, this implies that the coupling mechanism is not taking place through the Si substrate. The measured coupling also shows that the forward and backward coupling is reduced by approximately

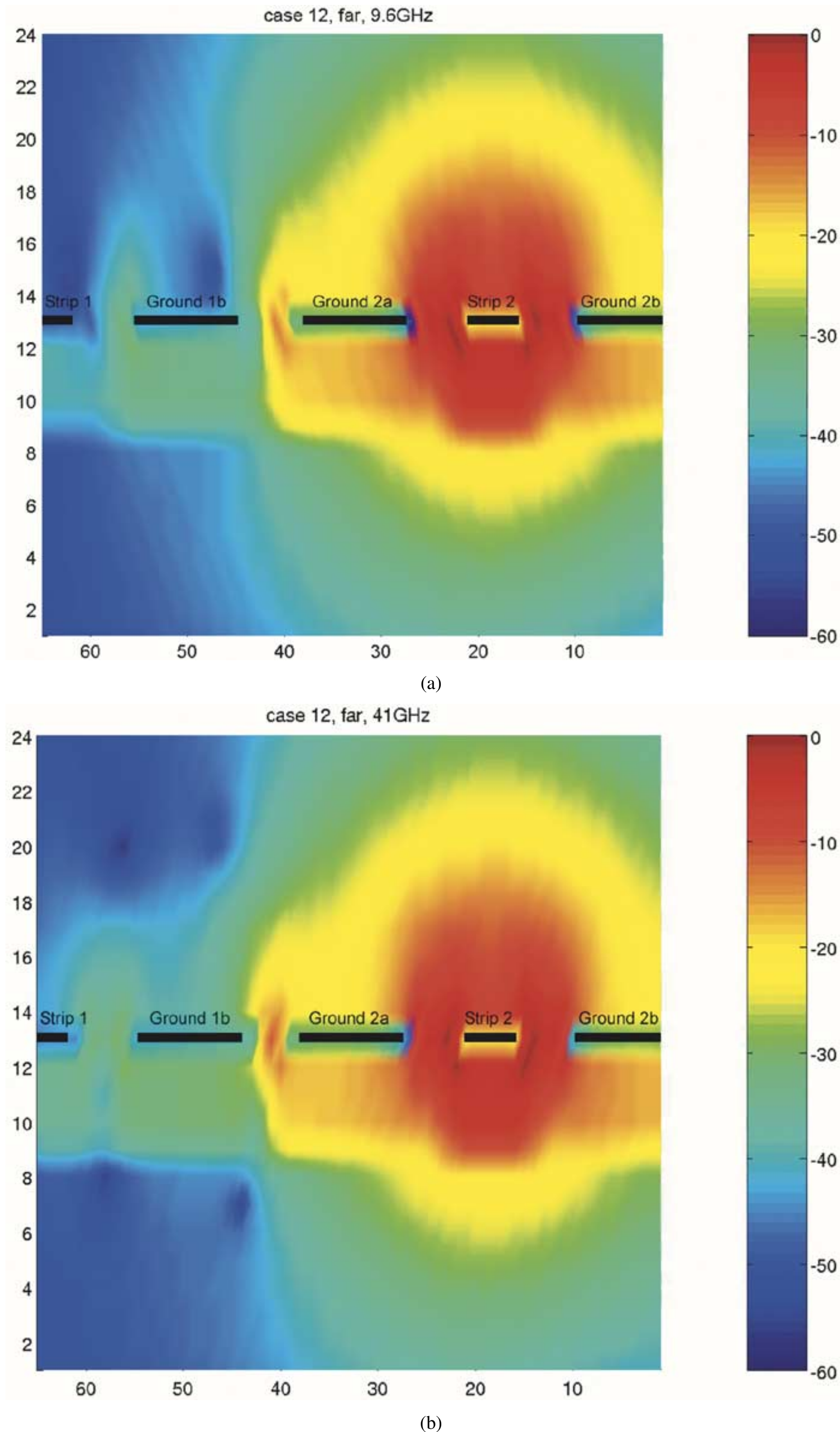

Fig. 9. Electric-field plots for the $S = 42$ μm, $W = 24$ μm, and $B = 84$ μm FGC line where $D = 12$ μm. Field plots are taken at various frequencies. (a) 9.6 GHz. (b) 41 GHz.

10 dB across the entire frequency band when $D > 0$ for both FGC line geometries. This indicates that, for high-density RF circuits and packages, even a very small distance between adjacent FGC lines can yield a significant (over 10 dB) reduction in cross-coupling and isolation. Lastly, Figs. 5 and 6 show that as the distances B and C increase, both couplings reduce significantly. However, since real estate is of primary importance in high-density circuits and interconnects, $B = 2S$ provides an excellent compromise between small-size and low FGC line cross-coupling (less than -40 dB).

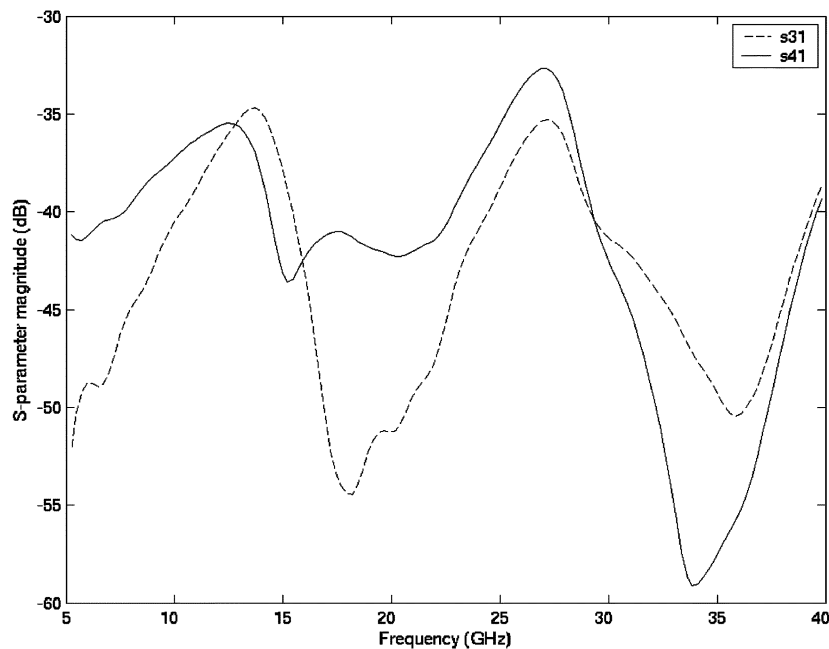

Fig. 10. FDTD determined amplitude of S-parameters for the FGC geometry with $S = 42$ μm, $W = 24$ μm, $B = 84$ μm, and $D = 6$ μm.

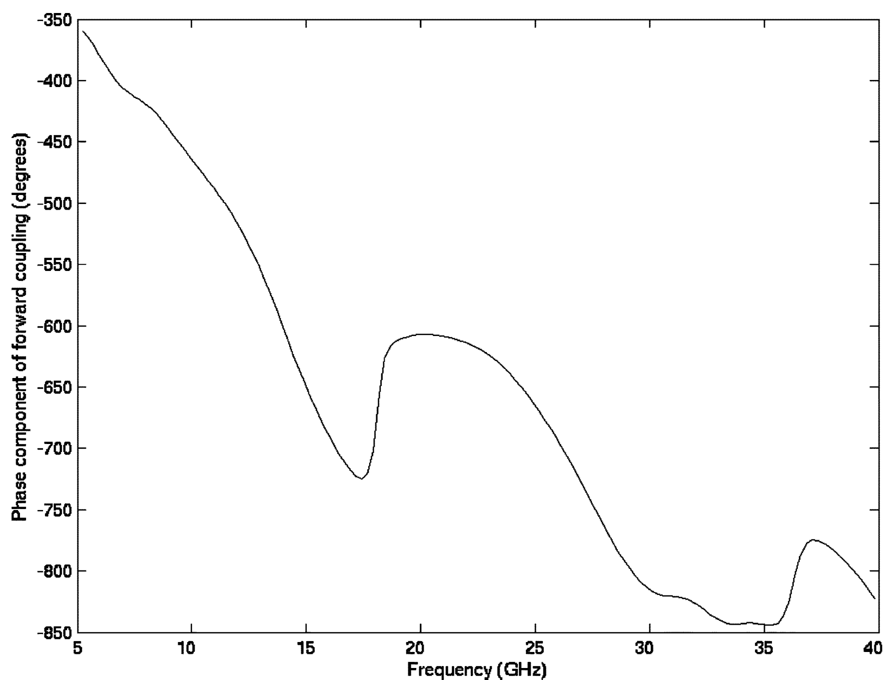

Fig. 11. FDTD determined phase of S_{31} for the for the FGC geometry with $S = 42$ μm, $W = 24$ μm, $B = 84$ μm, and $D = 6$ μm.

V. Theoretical Analysis

To understand the physics behind the coupling in the different structures and the dips in measured S_{31} and S_{41} at specific frequencies for both high and low substrate resistivities, electric-field plots were generated from the ATHENA FDTD simulator for the coupled FGC lines with $S = 42$ μm, $W = 24$ μm, and $B = 84$ μm line on high-ρ silicon with the dielectric overlay, and these are shown in Figs. 7–9 for different values of line separation D. For each FGC line, the left- and right-hand-side metal ground planes were connected with 40-μm air bridges that were spaced every 1500 μm in a way similar to the measured setup. The simulated length of the lines was 7200 μm, which is close to the 7500 μm of the experimental geometry. Three different three-dimensional (3-D) simulations were performed for the calculation of the S-parameters of each geometry, namely, one for a thru line, one for an even-mode excited coupled geometry, and another for an odd-mode excited coupled geometry. The slope of the phase for S_{31} (and S_{41}) was used for the identification of the excitation frequencies for the parasitic modes. Two-and-one-half-dimensional (2.5-D) FDTD simulations were performed for each mode in order to identify the individual field pattern and provide intuition for the minimization of the crosstalk mechanisms. The cross-sectional electric-field

plots of Figs. 7–9 span the area of the right FGC line ("exciting" line) and half of the signal line and right ground plane of the left FGC line ("excited" line). These field plots illustrate the strength of the coupling fields from one FGC line (right) to the other (left) for different values of separation D. By observing the field magnitude in the slot of the excited FGC line (on the left-hand side of Figs. 7–9), it is seen that with $D = 0$ μm, the coupling between FGC lines is noticeably stronger than the other two cases with $D > 0$. The reason for this increased coupling when $D = 0$ is attributed to surface currents developed on the bottom of the common ground plane that are broken when $D > 0$. For $D > 0$, the slot between the two ground planes stops the direct flow of current from the exciting to the excited FGC line through the ground planes and, thus, acts as a shield. However, Figs. 8 and 9 show a strong slotline type mode of approximately -15 dB between the two ground planes. This strong parasitic mode is the cause of the indirect coupling that was discussed in Section IV.

Since the ground planes of each FGC line are connected by air bridges (ground planes 1a and 1b and 2a and 2b are connected), the coupled FGC lines consist of a total of three metal structures when $D = 0$ and four metal structures when $D > 0$, which can support two and three independent quasi-TEM modes, respectively. One of the modes in each case is the desired CPW mode (note that we are assuming that the two FGC lines have the same geometry so each supports the same CPW mode). In Figs. 10 and 11, the magnitude and phase of the coupling determined by the FDTD analysis is plotted. It should be noted that the shape of Fig. 10 is close to the shape of Fig. 3(b). The nonmonotonic behavior of the S-parameters for $D > 0$, demonstrated for $D = 6$ μm in Fig. 10, can be attributed to the excitation of the two parasitic modes, the slotline mode ("Mode 1") between ground 2a of the exciting (right-hand side) FGC and ground 1b of the excited (left-hand side) FGC (simulated $\varepsilon_{\rm eff} \sim 2.50$) and the slotline mode ("Mode 2") between ground planes 2a and 2b of the exciting (right-hand side) FGC and the signal metal of the excited (left-hand side) FGC (simulated $\varepsilon_{\rm eff} \sim 2.90$). The higher $\varepsilon_{\rm eff}$ value of "Mode 2" can be attributed to the deeper penetration of the electric field inside the Si substrate due to the larger metal spacing. Fig. 11 shows the change of the slope of the phase of S_{31} around 19 and 35 GHz justifying this assumption. "Mode 2" is coupled first at around 19 GHz due to its higher $\varepsilon_{\rm eff}$ and "Mode 1" is coupled at around 35 GHz. Only weak surface modes have been observed with amplitudes that are significantly lower with respect to the two parasitic modes.

VI. Conclusions

This paper has shown for the first time that coupling between adjacent FGC lines on top of a silicon substrate with a polyimide overlay can be significantly reduced (10 dB or more) when the lines are separated by a distance as small as 6 μm for both high- and low-resistivity silicon wafers. Isolation values better than -40 and -30 dB were also demonstrated in both substrate cases for frequencies up to 25 and 50 GHz, respectively, for minute gaps between two FGC lines. These results can, therefore, be used as a new design guideline for high-density RF circuits and interconnects that utilize FGC lines on silicon substrates of various resistivity values. Measured results confirmed by theoretical simulations also show that the nature of the coupling is different for the FGC lines compared to TFMSs. Indeed, for small separations between adjacent FGC lines, coupling increases in a nonmonotonic fashion and exhibits various dips. Results presented in this paper also showed that for larger ground-plane widths and center-to-center FGC line distances, both forward and backward couplings are further reduced independently of the substrate resistivity. In addition, line crosstalk, in terms of forward and backward coupling values, is independent of the underlying silicon resistivity.

References

[1] G. Freeman, J. S. Rieh, B. Jagannathan, Z. Yang, F. Guarin, and A. Joseph, "Device scaling and application trends for over 200 GHz SiGe HBTs," in *Silicon Monolithic Integrated Circuits in RF Systems Topical Meeting Dig.*, Grainau, Germany, Apr. 9–11, 2003, pp. 6–9.

[2] J. Buechler, E. Kasper, P. Russer, and K. M. Strohm, "Silicon high-resistivity substrate millimeter-wave technology," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 1516–1521, Dec. 1986.

[3] C. Warns, W. Menzel, and H. Schumacher, "Transmission lines and passive elements for multilayer coplanar circuits on silicon," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 616–622, May 1998.

[4] W. Heinrich, J. Gerdes, F. J. Schmuckle, C. Rheinfelder, and K. Strohm, "Coplanar passive elements on Si substrate for frequencies up to 110 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 709–712, May 1998.

[5] A. Margomenos, K. Herrick, M. Herman, S. Valas, and L. Katehi, "Isolation in three-dimensional integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 25–32, Jan. 2003.

[6] R. Rasshofer, M. Thieme, and E. Biebl, "Circularly polarized millimeter-wave rectenna on silicon substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 715–718, May 1998.

[7] S. Yang *et al.*, "Characteristics of trenched coplanar waveguide for high-resistivity Si MMIC applications," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 623–631, May 1998.

[8] V. Milanovic, M. Ozgur, D. C. DeGroot, J. A. Jargon, M. Gaitan, and M. E. Zaghloul, "Characterization of broadband transmission for coplanar waveguides on CMOS silicon substrates," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 632–640, May 1998.

[9] G. Ponchak and A. Downey, "Characterization of thin film microstrip lines on polyimide," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 21, pp. 171–176, May 1998.

[10] G. Ponchak and L. Katehi, "Measured attenuation of coplanar waveguide on CMOS grade Si substrates with a polyimide interface layer," *Electron. Lett.*, vol. 34, no. 13, pp. 1327–1329, June 1998.

[11] J. Papapolymerou and G. Ponchak, "Microwave filters on a low resistivity Si substrate with a polyimide interface layer for wireless circuits," in *IEEE RFIC Symp. Dig.*, May 2001, pp. 125–128.

[12] K. Grenier, F. Bouchribal, D. Dubuc, P. Pons, J. Graffeuil, and R. Plana, "Novel technological solution to improve both Q factor and losses of passive circuits on low resistivity silicon," in *Silicon Monolithic Integrated Circuits in RF Systems Topical Meeting Dig.*, Grainau, Germany, April 9–11, 2003, pp. 115–117.

[13] S. Robertson, L. Katehi, and G. Rebeiz, "Micromachined W-band filters," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 598–606, Apr. 1996.

[14] G. Ponchak, A. Margomenos, and L. Katehi, "Low loss CPW on low resistivity Si substrates with a micromachined polyimide interface layer for RFIC interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 866–870, May 2001.

[15] G. Ponchak, E. Tentzeris, and J. Papapolymerou, "Coupling between microstrip lines embedded in polyimide layers for 3D-MMIC's on Si," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001, pp. 1723–1726.

[16] G. Ponchak, E. Dalton, A. Bacon, J. Papapolymerou, and E. Tentzeris, "Measured propagation characteristics of finite ground coplanar waveguide on silicon with a thick polyimide interface layer," in *Eur. Microwave Conf. Dig.*, Milan, Italy, Sept. 2002, pp. 167–170.

[17] G. Ponchak, L. Katehi, and E. Tentzeris, "Characterization of the coupling between adjacent FGC waveguides," *Int. J. Microcircuits Electron. Packag.*, vol. 20, no. 4, pp. 587–592, Fourth Quarter 1997.

[18] M. Riaziat, R. Majidi-Ahy, and I. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 245–250, Mar. 1990.

[19] G. Ponchak, J. Papapolymerou, and E. Tentzeris, "Coupling between finite ground coplanar waveguides embedded in polyimide layers for 3D-MMIC's on Si," in *Eur. Microwave Conf. Dig.*, London, U.K., Sept. 2001, pp. 25–29.

[20] K. C. Gupta, R.Ramesh Garg, I.Inder Bahl, and P.Prakash Bharitia, *Microstrip Lines and Slotlines*, 2nd ed. Norwood, MA: Artech House, 1996, pp. 375–404.

[21] D. A. Hill, K. H. Cavcey, and R. T. Johnk, "Crosstalk between microstrip transmission lines," *IEEE Trans. Electromagn. Compat.*, vol. 36, pp. 314–321, Nov. 1994.

[22] S. A. Schelkunoff and T. M. Odarenko, "Crosstalk between coaxial transmission lines," *Bell Syst. Tech. J.*, vol. 16, pp. 144–164, 1937.

John Papapolymerou (S'90–M'99–SM'04) received the B.S.E.E. degree from the National Technical University of Athens, Athens, Greece, in 1993, and the M.S.E.E. and Ph.D. degrees from The University of Michigan at Ann Arbor, in 1994 and 1999, respectively.

From 1999 to 2001, he was a faculty member with the Department of Electrical and Computer Engineering, University of Arizona, Tucson. During the summers of 2000 and 2003, he was a Visiting Professor with The University of Limoges, Limoges, France. In August 2001, he joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, where he is currently an Assistant Professor. He has authored or coauthored over 70 publications in peer reviewed journals and conferences. His research interests include the implementation of micromachining techniques and microelectromechanical system (MEMS) devices in microwave, millimeter-wave, and terahertz circuits and the development of both passive and active planar circuits on Si and GaAs for high-frequency applications.

Dr. Papapolymerou was the recipient of the 2002 National Science Foundation (NSF) CAREER Award, the Best Paper Award presented at the 3rd IEEE International Conference on Microwave and Millimeter-Wave Technology (ICMMT2002), Beijing, China (August 17–19, 2002), and the 1997 Outstanding Graduate Student Instructional Assistant Award presented by the American Society for Engineering Education (ASEE), The University of Michigan Chapter.

George E. Ponchak (S'82–M'83–SM'97) received the B.E.E. degree from Cleveland State University, Cleveland, OH, in 1983, the M.S.E.E. degree from Case Western Reserve University, Cleveland, OH, in 1987, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 1997.

In 1983, he joined the staff of the Communication Technology Division, National Aeronautics and Space Administration (NASA) Glenn Research Center, Cleveland, OH, where he is currently a Senior Research Engineer. From 1997 to 1998 and 2000 to 2001, he was a Visiting Lecturer with Case Western Reserve University. He has authored and coauthored over 90 papers in refereed journals and symposia proceedings. His research interests include the development and characterization of microwave and millimeter-wave printed transmission lines and passive circuits, multilayer interconnects, uniplanar circuits, microwave microelectromechanical (MEMS) components, and microwave packaging. He is responsible for the development of GaAs, InP, and SiGe MMICs for space applications.

Dr. Ponchak is a senior member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) and a member of the International Microelectronics and Packaging Society (IMAPS). He was the recipient of the Best Paper of the ISHM'97 30th International Symposium on Microelectronics Award. He was editor of a Special Issue on Si MMICs of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He founded the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems and served as its chair in 1998 and 2001 and its digest editor in 2000 and 2003. In addition, he has chaired many IEEE MTT-S International Microwave Symposium workshops and special sessions. He is a member of the IEEE MTT-S International Microwave Symposium (IMS) Technical Program Committee (TPC) on Transmission Line Elements and serves as its chair. He is a member of the IEEE MTT-S Administrative Committee (AdCom) Membership Services Committee.

Edan Dalton received the B.S. degree in electrical engineering from Auburn University, Auburn, AL, in 2000, and is currently working toward the Ph.D. degree in electrical engineering at the Georgia Institute of Technology, Atlanta.

He is currently a Research Assistant with the ATHENA Research Group, Georgia Institute of Technology, and works closely with the NSF Packaging Research Center and the Yamacraw Research Center of the State of Georgia. His main research interest is time-domain electromagnetic simulation techniques with an emphasis on finite-difference time-domain (FDTD) and multiresolution time-domain (MRTD) modeling, and hybrid techniques. He also researches multilayer RF packaging and electromagnetic interference modeling.

Andrew Bacon received the B.S. (with high honors) and M.S. degrees from the Georgia Institute of Technology, Atlanta, in 2001 and 2002, respectively, both in electrical and computer engineering.

He was with the MircTech Research Group, George Institute of Technology, where he was involved with folded coplanar-waveguide slot antennas and other coplanar structures. He was also involved with polyimide processing and integration of RF circuitry onto CMOS grade silicon. He is currently an Engineer with Northrop Grumman, Baltimore, MD.

Manos M. Tentzeris (SM'03) received the Diploma degree in electrical and computer engineering from the National Technical University of Athens, Athens, Greece, in 1992, and the M.S. and Ph.D. degrees in electrical engineering and computer science from The University of Michigan at Ann Arbor, in 1993 and 1998, respectively.

He is currently an Associate Professor with School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta. During the summer of 2002, he was a Visiting Professor with the Technical University of Munich, Munich, Germany. He has authored or coauthored over 120 papers in refereed journals and conference proceedings and six book chapters. He has helped develop academic programs in highly integrated packaging for RF and wireless applications, microwave MEMs, SOP-integrated antennas and adaptive numerical electromagnetics (FDTD, multiresolution algorithms). He is the Georgia Tech NSF-Packaging Research Center Associate Director for RF Research and the RF Alliance Leader. He is also the Leader of the Novel Integration Techniques Sub-Thrust of the Broadband Hardware Access Thrust of the Georgia Electronic Design Center (GEDC) of the State of Georgia.

Dr. Tentzeris is member of the Technical Chamber of Greece. He was the 1999 Technical Program co-chair of the 54th ARFTG Conference, Atlanta, GA. He is the vice-chair of the RF Technical Committee (TC16) of the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society. He was the recipient of the 2003 IEEE CPMT Outstanding Young Engineer Award, the 2002 International Conference on Microwave and Millimeter-Wave Technology Best Paper Award (Beijing, China), the 2002 Georgia Tech-Electrical and Computer Engineering (ECE) Outstanding Junior Faculty Award, the 2001 ACES Conference Best Paper Award, the 2000 NSF CAREER Award, and the 1997 Best Paper Award, International Hybrid Microelectronics and Packaging Society.