Integrated RF Architectures in Fully-Organic SOP Technology

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***Abstract*—Future wireless communications systems require better performance, lower cost, and compact RF front-end footprint. The RF front-end module development and its level of integration are, thus, continuous challenges. In most of the presently used microwave integrated circuit technologies, it is difficult to integrate the passives efficiently with required quality. Another critical obstacle in the design of passive components, which occupy the highest percentage of integrated circuit and circuit board real estate, includes the effort to reduce the module size. These issues can be addressed with multilayer substrate technology. A multilayer organic (MLO)-based process offers the potential as the next generation technology of choice for electronic packaging. It uses a cost effective process, while offering design flexibility and optimized integration due to its multilayer topology. We present the design, model, and measurement data of RF-microwave multilayer transitions and integrated passives implemented in a MLO system on package (SOP) technology. Compact, high Q inductors, and embedded filter designs for wireless module applications are demonstrated for the first time in this technology.**

***Index Terms*—Bandpass filter, CPW–microstrip transition, high-Q inductors, lowpass filter, multilayer organic, system on package.**

I. Introduction

EMERGING applications in the RF/microwave/millimeter wave regimes require miniaturization, portability, cost, and performance as key driving forces in this evolution. Investigations on the system on package (SOP) approach for module development [1] have become a primary focus due to the real estate efficiency, cost-savings and performance improvement potentially involved in this integral functionality.

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In most of the presently used RF front-end architectures, complete system integration has not been achieved. External components such as the antenna and passives used for impedance matching, for instance, are still needed. Another area of concentration includes the design of passive components to reduce the overall module size. Design flexibility and optimized integration can be achieved with multilayer substrate technology in which free vertical real-estate is taken advantage of. In this configuration, an antenna, for example, may be implemented on the same package as embedded passives allowed by the various layers of metals and dielectrics.

As a next step in the realization of completely integrated wireless communication front-end systems, we demonstrate the capability of embedding passive components, including compact high Q inductors in MLO process technology for RF and microwave applications. In addition to individual passive device implementation, SOP technology can also be used to integrate complete passive RF front-end functional building blocks, such as filters [2]. The high quality factor of passive components possible in this process allows for successful integration of these RF filters, for example.

II. SOP Technology

SOP technology offers the advantages of low cost and high performance materials while ultimately providing a complete packaging solution for RF modules. High performance can be achieved while addressing the issues of cost and module size. Various highly intergrable multilayer technologies such as low [3] and high temperature co-fired ceramic (LTCC and HTCC) and MCM-D [4] have been the most suitable technologies for implementing a complete SOP solution. However, organic process technology [5] is currently being studied to achieve complete SOP solutions. Advantages of SOP include: lower cost and design flexibility due to the use of embedded high Q passives, minimization of loss and parasitic effects due to the reduction in the number and lengths of interconnections and reduction of module size due to the multilayer topology. The more mature LTCC process has been heavily studied and has produced optimized helical inductor with $L = 1.4$ nH, $Q\max = 100$ and SRF of 8 GHz [6]. Highly integrated LTCC based transmitter modules using GaAs MESFET MMICs for C band OFDM [7] and Ku band satellite applications [8] have also been presented. In this paper, we present compact inductors with high Q in the microwave frequency range. The compact

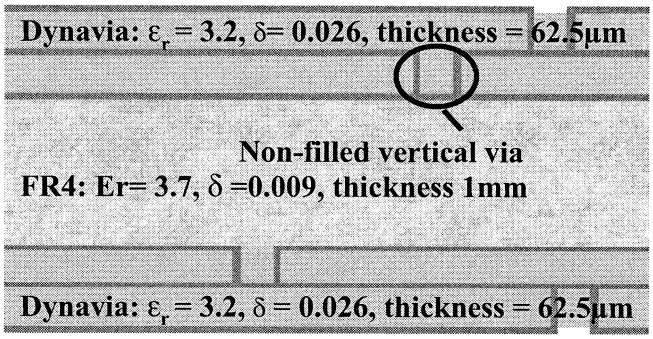

Fig. 1. Cross section of MLO technology for SOP integration used in this study.

CPW inductor presented demonstrates a measured Q of as high as 182 and self-resonant-frequency (SRF) as high as 20 GHz. This represents the highest reported Q in its frequency range to date in a multilayer topology including MCM [9], LTCC [6], and MCM-L [10]. We also demonstrate how a fully integrated MLO-based transmitter module incorporating two MMICs, a miniaturized square patch resonator bandpass filter with inset feeds and a lifted slot antenna (LSA) can be achieved.

III. Multilayer Organic Packaging

A multilayer packaging process using an organic material developed by Georgia Institute of Technology's Packaging Research Center offers the potential as the next generation technology of choice for SOP for RF-wireless, high speed digital and RF-optical applications. The current SOP configuration is shown in Fig. 1. It represents a low-temperature, large area, and reliable assembly process. Volume insulation resistance at 65 °C/90% RH is 1.5 E + 13 Ω. It incorporates low cost materials and processes consisting of a core substrate laminated with two thin organic layers. The core substrate is a 1 mm (40 mil) thick double-sided FR-4 having $\tan\delta = 0.009$ and $\varepsilon_r = 3.7$. The Shipley/Morton Dynavia 2000 dry film epoxy layers has a $\tan\delta = 0.026$, $\varepsilon_r = 3.2$ and are 62.5 μm each. The integral passive components are fabricated within the wiring structure of the SOP module, which consists of a three metal layer structure including two layers of high density wiring metallization and two micro via levels. 10–18 μm copper metallization and 100 μm diameter microvia process are used for this multilayer interconnection structure. The minimum metal line width and spacing is 25 μm for the top two metal layers. Using this topology, high density hybrid interconnect schemes as well as various compact passive structures, including inductors, capacitors and filters have also been designed and measured [10].

IV. CPW–Microstrip Transitions

A hybrid CPW–microstrip transition has been designed and tested. The CPW–microstrip high-density transition scheme allows flexibility in circuit design, which results in reduction in size of electronic devices while overcoming space restrictions. The CPW line is fabricated on FR-4 board to allow MMICs or surface-mount packaged chips to be attached through flip-chip or soldering process, respectively. Both microstrips are established on the laminate layer through via transitioning

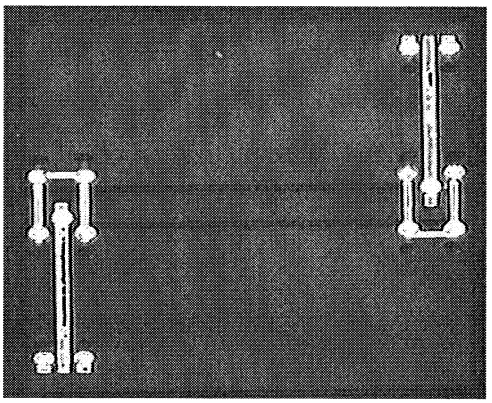

Fig. 2. CPW–microstrip transition with via bridge.

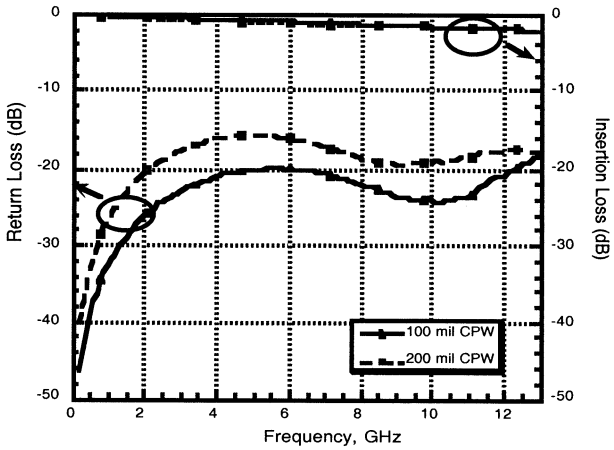

Fig. 3. Return and insertion loss of CPW–microstrip transition.

from CPW to the microstrip signal lines. Embedded R, L, and Cs can be fabricated in this microstrip configuration [11]. Via bridges, seen in Fig. 2, were then added surrounding the transition to increase the capacitive effects of the transition and improve the return loss. The CPW–microstrip transition measurements were performed using air-coplanar probes after an LRM calibration. A return loss better than 20 dB to 12 GHz and an insertion loss of 1.7 dB at 12 GHz for the 100 mil CPW are demonstrated in Fig. 3. As the length of the CPW increases the performance deteriorates; however, in the actual module, the CPW length is kept short since it only serves as MMIC attachment pads. The via bridges were added from the top metal to the CPW grounds, making up to a 35% improvement in S11 compared to transition without bridges.

V. Multilayer Inductors

Simple one to six-turn inductors are designed and measured. The Q and SRF of an MLO inductor can be analyzed using a lumped element circuit model for a one-port inductor shown in Fig. 4. The model consists of an ideal L in series with a resistor Rs to account for the conductor and via loss. The dielectric loss, the substrate capacitance, and coupling capacitance between turns are represented by R_p, C_s, and C_c, respectively. Since C_s and C_c are in parallel, the two can be combined together into a single capacitor C. The Q is measured by taking the

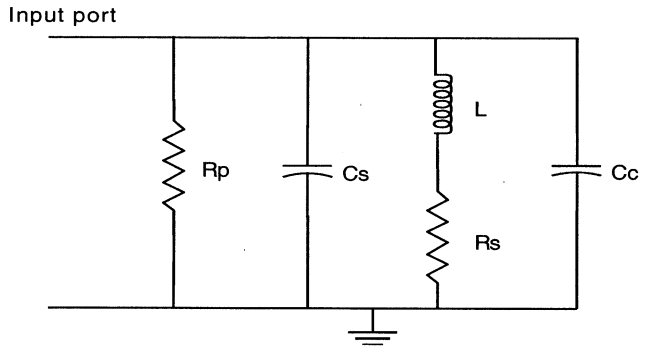

Fig. 4. Lumped element circuit model for MLO inductor.

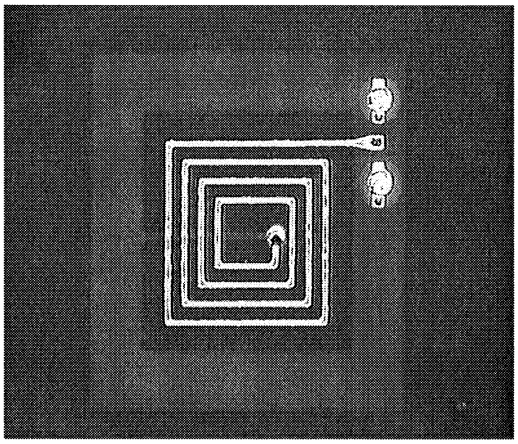

Fig. 5. Photograph of simple four-turn inductor implemented in HGP configuration.

TABLE I
SUMMARY OF LUMPED ELEMENT VALUES USED IN MLO INDUCTOR MODEL

Type	L(nH)	Rs(Ω)	Rp(kΩ)	C(pF)
FGP	3.3	.6	7	.08
HGP	4.5	.35	10	.074

ratio of the imaginary part to the real part of the input impedance of the inductor obtained from a one-port S-parameter measurement. It can be shown, however, that this is equivalent to the definition of Q, which is the ratio of the energy stored compared to the energy loss. The analytical expression of the inductor Q of the circuit model in Fig. 4 is given by [12]

$$Q = \left[\frac{\omega L_s}{R_s}\right]\left[\frac{R_p}{R_p + R_s\left(1+\left(\frac{\omega L_s}{R_s}\right)^2\right)}\right] \cdot \left[1 - \frac{R_s^2 C}{L_s} - \omega^2 L_s C\right].$$

In general for a simple turn inductor, as the area increases with the number of turns, R_s, C_s, and C_c increases while R_p decreases. This topology therefore decreases in Q and SRF significantly as the number of turns increase. With a hollow ground plane (HGP) configuration, higher Q and effective inductance, L_{eff} can be achieved while maintaining the size of the inductor footprint. The effective inductance is the total inductance seen

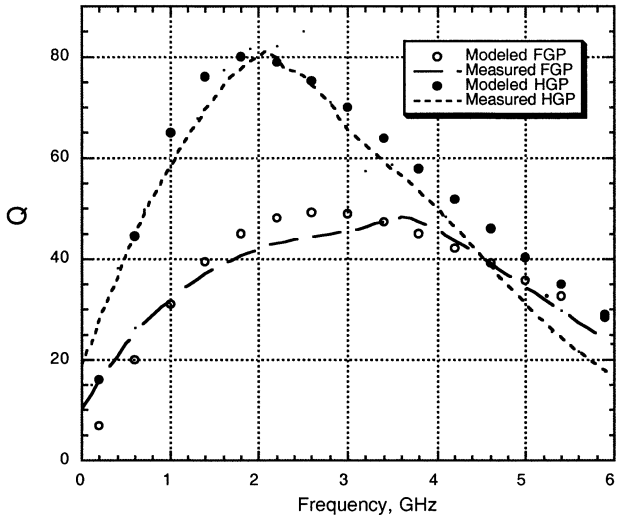

Fig. 6. Measured and modeled Q factor of a FGP and HGP implemented two-turn spiral inductor.

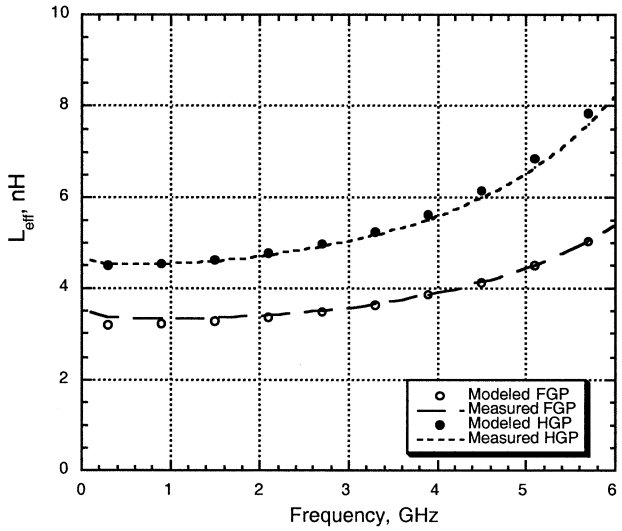

Fig. 7. Measured and modeled L_{eff} of a FGP and HGP implemented two-turn spiral inductor.

at the input port of the inductor and is obtained by taking the ratio of the imaginary part of the input impedance to the angular frequency, ω. The HGP configuration creates a ground plane opening under the footprint of the inductor, which decreases shunt parasitic capacitance and negative mutual coupling caused by eddy current in the ground plane resulting in higher Q and L_{eff}. A simple four-turn inductor implemented in HGP configuration is shown in Fig. 5. Another benefit of the HGP configuration is that the L_{eff} can be adjusted by increasing or decreasing the shunt parasitic capacitor, C_s and negative mutual coupling due to the ground plane. This is achieved by decreasing or increasing the area of the hollow ground plane opening, respectively. Decreasing the HGP opening increases C_s therefore canceling part of the inductance. Increasing the opening reduces C_s and increases L_{eff}.

The proposed inductor model of the full ground plane (FGP) and HGP simple two-turn inductor shows an excellent correlation to the measured results. The values of L, Rs, Rp, and C for

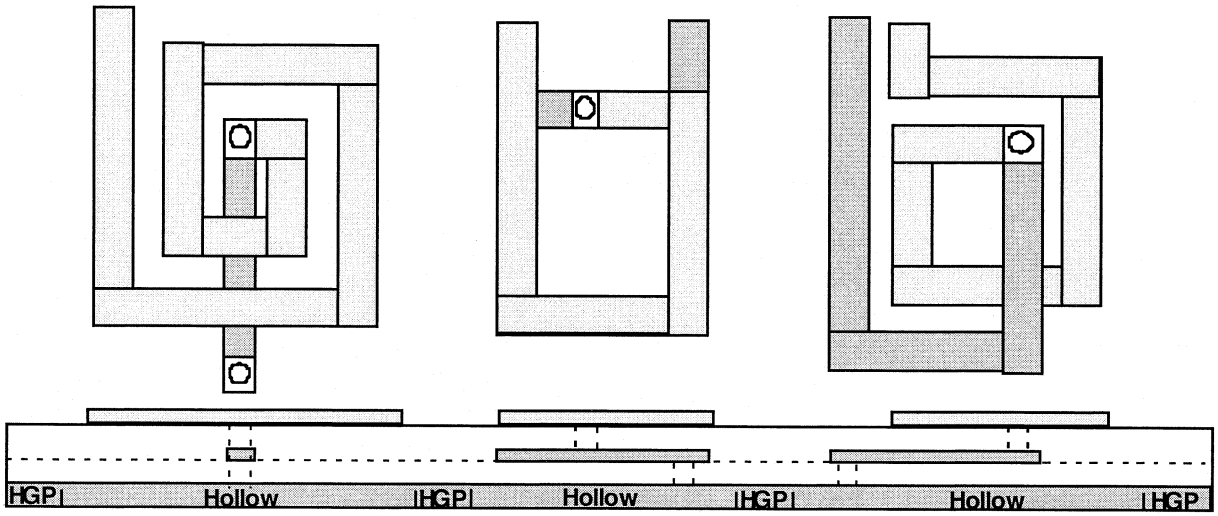

Fig. 8. Top and cross sectional view MLO HGP simple, cascade, and series two-turn inductors.

TABLE II
SUMMARY OF MEASURED MLO INDUCTOR PERFORMANCE

Type	Qmax	L_{eff}(nH)	SRF (GHz)	Area (mm^2)
HGP simple 2 turn	81	4.5	9	1 x 1
HGP series 2turn	122	2.5	10	.95 x .86
HGP cascade 2turn	165	3.4	11.5	.6 x .6

each topology shown in Table I are optimized to match the measured Q and L_{eff}. This correlation, as well as the HGP improvement, can be seen in Fig. 6, which shows the measured, and modeled Q of a FGP and HGP simple two-turn inductor. The HGP improvement and increase in L_{eff} of a simple two-turn inductor can be seen in Figs. 6 and 7, respectively. The Q was improved by approximately 60%. As the number of turns increase, the HGP configuration can result in a significantly higher improvement in Q based on the proportionally larger reduction in parasitic capacitance. A three times improvement in Q was achieved for a simple six turn inductor with HGP implementation [13], despite the lower Q due to the thinner dielectric layers (25 μm) used in a previous tape out.

In addition to the commercial simulator used previously [14], finite-difference time-domain (FDTD) analysis is applied to the modeling of the HGP simple two-turn inductor. The correct characterization of these components requires that they be examined over the entire frequency band of operation. Time domain techniques are well suited for this requirement as the time domain results from a single simulation can be used to determine the response over an arbitrary frequency band through the use of a Fourier transform. This code uses a variable grid and has been parallelized to increase efficiency and reduce execution time. The Q and SRF of the HGP two-turn inductor were verified using this FDTD technique.

High Q at the frequency range of interest can be obtained by designing compact CPW inductors and HGP series and cascade inductors using MLO process technology. The CPW spiral inductor has the same advantages of HGP inductors; in addition, it avoids via losses, has reduced dielectric losses and increased SRF. Also the thick copper metallization in the packaging process makes it possible to get a very high Q. As a result higher Q and L_{eff} can be achieved. The measured Q factor of the CPW inductor is as high as 182 and SRF as high as 20 GHz with a 0.91 mm diameter. The two-turn series inductor is designed as one continuous turn similar to the simple two-turn inductor; however, the turn on the second layer is offset from the turn on the top layer. This offset helps decrease the coupling capacitance, Cc between the turns and improves SRF. In the cascade inductor configuration, the top metal and bottom metal spiral separately and are connected at the center of the spiral. The top and bottom spiral are overlapped and strongly coupled yielding an impressive Q and effective inductance, L_{eff}. The top and side views of HGP simple cascade and series two-turn inductors are depicted in Fig. 8. The measured results are summarized in Table II.

VI. EMBEDDED FILTERS

Two front-end RF filters presented here were designed in various topologies for wireless module applications. The first MLO filter is a second order Bessel lumped element LPF with cutoff frequency at 750 MHz. For RF and low microwave applications, this filter can be implemented by combinations of capacitive and inductive lumped passive components. It is used to filter 1 Gb/s header data stream in a 10 Gb/s OSCM system operating at 14 GHz. Fig. 9 shows the second order Bessel lumped element lowpass filter with cutoff frequency at 750 MHz. The simulated and measured return loss and insertion loss are shown in Fig. 10. The size of this structure is 5.7 $\times$ 4.3 mm^2.

The second MLO filter is a BPF designed for C band applications and has a size of 9.3 $\times$ 9.3 mm^2. It consists of a square

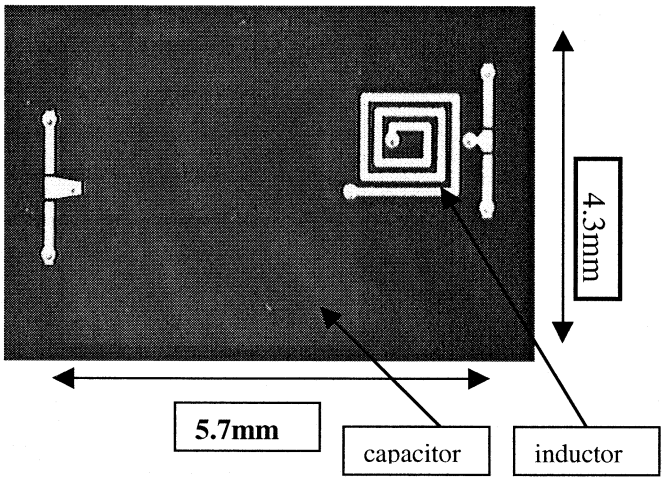

Fig. 9. Photograph of MLO lumped element filter.

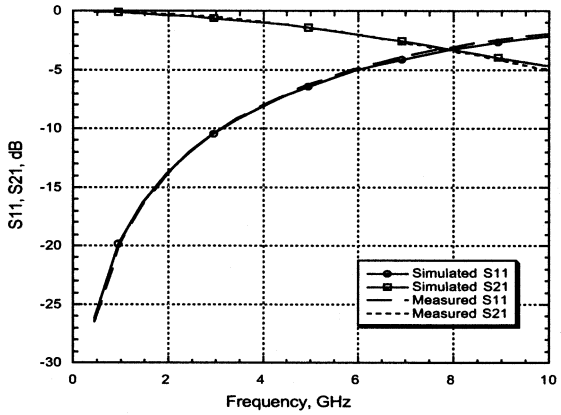

Fig. 10. Measured and simulated S11, S21 of lumped element filter.

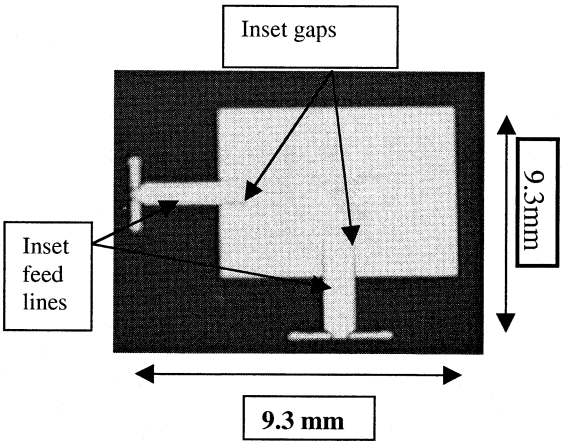

Fig. 11. Photograph of MLO C-band BPF.

patch resonator [15] with inset feed lines (see Fig. 11). The inset gaps act as small capacitors and cause the filter to have a pseudo-elliptic response with transmission zeros on either side of the passband. This structure also has a tunable bandwidth. The length of the insets and the distance between them are the main controlling factors, effectively setting the size of the mode-splitting perturbation in the field of the resonator. The length of the feed lines is determined by the input and output matching requirements. Fig. 12 shows a center frequency of 5.8 GHz, bandwidth of 1.5 GHz and a minimum insertion loss of 3 dB. This BPF is implemented in a fully integrated MLO transmitter module, which includes a LSA for WLAN applications. The MMIC chips used are a C-band upconverter MMIC with excellent LO and image rejection as well as wideband operation along with a PA MMIC fabricated in a commercial GaAs MESFET process. This design realizes a compact highly integrated transmitter module suitable for the low cost network interface card (NIC), IEEE 802.11a WLAN applications in 5–6 GHz frequency band. The BPF is inserted between the upconverter MMIC and the PA to reject the spurious signals generated by the mixer. The LSA, with vertical feed to reduce feed loss and pattern distortion, was designed for 5.8 GHz and has a gain of 3.7 dBi and bandwidth 14% [16].

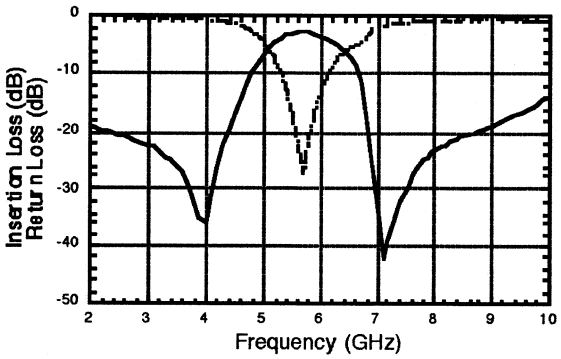

Fig. 12. S11, S21 of MLO C-band BPF.

VII. Conclusion

In this paper, we have demonstrated integrated RF architectures implemented in MLO process technology to achieve a complete packaging solution for RF modules. We have reported the lumped element electrical model and measured results of embedded high Q extremely compact inductor designs. The hollow ground plane (HGP) implementation demonstrated a 60% increase in Q. Embedded filter designs for various wireless module applications are achieved. A lowpass filter (LPF) with a cutoff frequency at 750 MHz and bandpass filter (BPF) with center frequency 5.8 GHz and 1.5 GHz bandwidth are highlighted. The C-band transmitter module including an integrated BPF and lifted slot antenna (LSA) is currently being fabricated. All components have been simulated using a commercial method of moment (MoM) simulator [17].

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