3D Glass Package-Integrated, High-Performance Power Dividing Networks for 5G Broadband Antennas

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***Abstract*—This paper demonstrates package-integrated power dividers with footprint smaller than the free-space wavelength corresponding to the operating frequency of 28 GHz band for 5G Antenna-in-Package (AiP), by utilizing precision low-loss redistribution layers (RDL) on glass substrates for highly-integrated mixed-signal systems. Two configurations of power dividers with two-way and three-way equal power split are modeled, designed and fabricated on glass substrates with thin-film build-up layers. This approach combines the benefits of ceramic and low-loss polymers for electrical performance, and silicon-like dimensional stability of glass for precision panel-scale patterning. Multilayered RDL with sub-20 micron features are utilized to design innovative power divider topologies with benefits in terms of low added insertion loss (<0.8-dB) and minimal phase-shift between the output ports, due to high precision of distributed transmission lines and through panel vias (TPVs). These power dividing networks depict upto 25% lower added insertion loss as compared to similar structures on fine pitch InFO RDL. The power dividers are also configured as 2×1 and 3×1 antenna arrays using Yagi-Uda antennas which cover the entire 28 GHz 5G band. The performance of power dividers as well as corresponding antenna arrays shows an excellent correlation between simulated and measured results.**

***Index Terms*—5G and mm-wave; small-cell; RF; power divider; T-junction; Yagi-Uda; antenna array; semi-additive process**

I. Introduction

The millimeter-wave (mm-wave) packaging technologies along with embedded antenna-in-package (AiP) is one of the vital contributors for the realization of high data-rate wireless communication. Significant momentum has been building up around the implementation of next generation of networks, namely 5G mobile communication systems, which are rumored to be commercially available to the end-users by 2020 [1–4]. For developing 5G wireless networks, the objectives include higher data-rate, higher capacity, high quality-of-service (QoS) low end-to-end latency, massive multiple-input multi-output (MIMO) capability and reduced cost [5], [6]. Millimeter-wave beam-forming is one of the most active areas in pursuit of compact, efficient and low-cost end-user devices as it is one of the key enabling technologies for 5G infrastructure such as small-cell and base-stations [7–10].

Due to higher free-space loss of mm-waves, high directivity and beam-steering of antennas becomes an inevitable requirement to enable a stronger and reliable wireless 5G connection. With the trend shifting towards package-integrated antennas, integrating a power dividing network with the antenna array in a package becomes extremely important as the power delivery to antennas operating at different bandwidths need to have minimal phase-shift [10]. Power dividers can be integrated either in the same metal layer or in the metal layer underneath the antenna array, depending primarily upon the complexity of the system as well as the chosen structure for power divider. Typical structures are based on microstrip, conductor-backed coplanar waveguide (CBCPW) or stripline [11–13]. Since the target layer is the top metal, microstrip structure is chosen for this demonstration as shown in Fig. 1.

A range of innovative substrate technologies have been explored for mm-wave antenna design. Antenna arrays have been demonstrated on state-of-the-art substrate technologies which include organic laminates, low-temperature co-fired ceramic (LTCC), integrated fan-out redistribution layer (InFO-RDL) and glass [14–18]. Antenna performance need to be optimized regardless of the substrate type in terms of desired bandwidth, gain and radiation pattern. Antenna-chip-package co-design also dictates the size of the antenna array, optimum material properties for interconnects as well as thermal and mechanical considerations. LTCC is limited by its high cost and scalability to large panels whereas organic substrates take

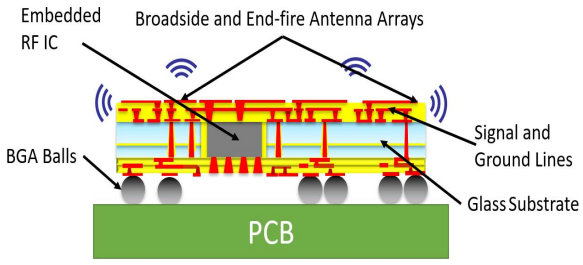

Figure 1. Illustration of an antenna-in-package module

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advantage of their low cost and scalability. However, they fall short in processability due to panel-scale warpage and reliability issues. InFO has challenges in use of epoxy molding compound and co-efficient of thermal expansion (CTE) mismatch with silicon dies. Glass-based packages are emerging as competitors to realize mm-wave technologies because of superior dimensional stability, availability in large-area low-cost panels, ability to form fine-pitch through-vias, stability to temperature and humidity, and matched coefficient of thermal expansion (CTE) with devices along with low dielectric loss compared to silicon and mold compounds used in fan-out packages.

In this paper, 3D package-integrated, equal-split power dividing networks with footprint smaller the free-space wavelength at the operating frequency of 28 GHz (24.5-29.5 GHz, FBW=18.51%) bands for 5G applications. Two power divider configurations: two- and three-way, are modeled, designed and fabricated on thin-film build-up layers on ultra-thin laminated glass substrate. The power dividers are connected with Yagi-Uda antennas to demonstrate their effectiveness. Utilizing glass core combines the benefits of ceramic or low-loss polymers for electrical performance, and silicon-like dimensional stability of glass for precision panel-scale patterning. Multilayered RDL are utilized to design innovative power divider topologies with benefits in terms of low added insertion loss, wide-bandwidth and minimal phase-shift. These power dividing networks depict upto 25% lower added insertion loss as compared to similar structures on fine pitch InFO RDL [16].

This paper is organized as follows: An introduction to the motivation and applications of this research is given in Section-1. The materials stackup and design techniques for the demonstration of power dividers is discussed in Section-2 followed by the detail of fabrication process in the Section-3. Finally, a comparison of simulated and measured results is given in Section-4.

II. Material Stackup, Modeling and Design Procedure of Power Dividers

A. Material Stackup

In this section, the material stackup and design procedure of power dividers is discussed. The microstrip structure is chosen for power dividers with the intent of integrating them into a module on the top metal layer, along with the antennas. The material stackup is shown in Fig. 2.

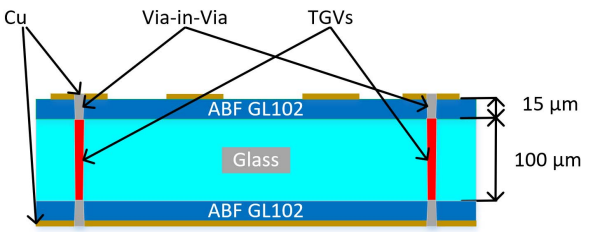
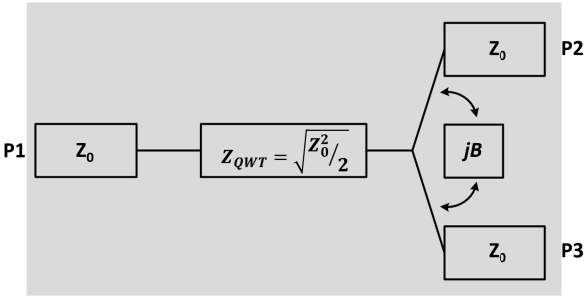


Figure 2. Material stackup for demonstration of power dividers

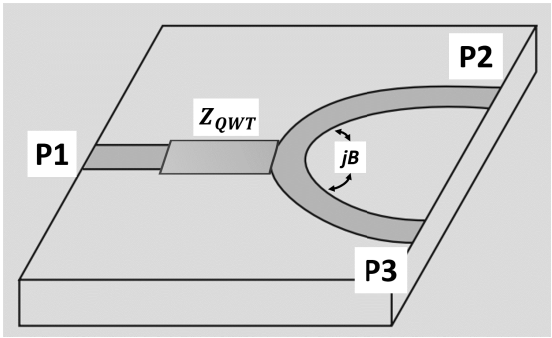
The material stackup consists of ultra-thin 100-μm EN-A1 glass substrate from Asahi Glass Co., (AGC) laminated with 15-μm Ajinomoto ABF GL102 on both sides. The electrical properties of the glass substrate are as follows: dielectric constant (Dk) = 5.4 and loss tangent (Df): 0.005 at 10 GHz. Similarly, the electrical properties of ABF GL102 are: Dk = 3.3 and Df = 0.0044 at 5.8 GHz and it has stable properties upto 50 GHz [19–21]. The desired copper thickness for the microstrip power divider structures is targeted to be 8-μm. The skin-depth at the highest operating frequency of 29.5 GHz is approximately 0.38-μm. The copper thickness of traces gives enough room to conveniently fabricate the microstrip transmission lines with decent power handling capabilities while keeping the conductor thickness more than five times of skin-depth for low-loss applications. The through-glass via (TGV) diameter is set to 100-μm, whereas the via-in-via diameter is adjusted accordingly. The minimum center-to-center via pitch is 450-μm. This material stackup is used in simulation using ANSYS High Frequency Structure Simulator (HFSS) for both power dividers in this demonstration.

B. Power Divider Design

The transmission line modeling of a power divider is based on a T-junction, as shown in the Fig. 3. Another usual choice of power divider is Wilkinson power divider as it is advantageous in terms of providing isolation between the output ports [22]. However, it can be disadvantageous for small packages as it requires a lumped resistor. Generally, there can be fringing



(a)



(b)

Figure 3. A T-junction power divider with a matching quarter-wave transformer (a) schematic, and (b) an example microstrip realization

fields in a T-junction, especially in a microstrip configuration, and higher order modes that are associated with the discontinuity at the junction of the three transmission lines. This can lead to stored energy, donated by lumped susceptance, *B*. Since the divider is lossy, it can be matched to all ports using a quarter wave transformer. Looking into the junction, the input admittance is seen as:

$$Y_{in} = jB + \frac{1}{Z_2} + \frac{1}{Z_3} = \frac{1}{Z_1} \tag{1}$$

where Z_n indicate impedance of the respective transmission line attached to the port n (n=1, 2, 3,...). In case of low-loss transmission lines, the characteristic impedance (Z_0) of transmission lines can be assumed to be real, equating *B* to zero. Thus, (1) transforms into (2):

$$\frac{1}{Z_1} = \frac{1}{Z_2} + \frac{1}{Z_3} \tag{2}$$

In practicality, *B* is not negligible but it can be compensated by either some discontinuity compensation or a reactive tuning element. Often, the impedance of output networks is adjusted as such to cancel out *B* over a narrow or a wide frequency range.

The power dividing networks designed for this demonstration are equal-split two- and three-way power dividers. For both cases, the characteristic impedance of the input and output lines is set at 50 Ω. Looking into the transmission line junction of the two-way network, two 50 Ω impedances are seen in parallel, making an effective impedance of 25 Ω. The input transmission line has an impedance of 50 Ω which is matched to the 25 Ω impedance using a quarter-wave transformer. Similarly, the three-way equal-split power divider has an impedance of 16.67 Ω looking into the junction of transmission lines and it is matched to the input impedance of 50 Ω using an appropriate quarter-wave transformer. This transformer also helps in countering the lumped susceptance *B* at the junction of the power divider. The distance between output ports is adjusted in reference to the dimensions of Yagi-Uda antennas and the required spacing between them for antenna arrays. The ideal spacing between array elements is usually half of the free-space wavelength (λ_0).

Since the material stackup for this demonstration consists of three dielectric layers sandwiched together as shown in Fig. 4, it is imperative to find the effective dielectric permittivity (ε_{rc}) of this stackup. The dielectric constants of each layer are donated by ε_n where n is the number of layers (n=1, 2, 3,...). It is expressed using the following set of equations in which h_n, h_{n-1},...h_1 represent the height of individual layer starting from the top and ε_n, ε_{n-1},...ε_1 correspond to the complex relative permittivity of the respective dielectric layer [23], [24]:

$$\varepsilon_{rc} = \frac{\mid d_1 \mid + \mid d_2 \mid + \mid d_3 \mid}{\mid \frac{d_1}{\varepsilon_1} \mid + \mid \frac{d_2}{\varepsilon_2} \mid + \mid \frac{d_3}{\varepsilon_3} \mid} \tag{3}$$

for $h_n+h_{n-1}+...+h_1 \simeq \lambda/10$.

$$d_1 = \frac{K(k_1)}{K'(k_1)} \tag{4}$$

$$d_2 = \frac{K(k_2)}{K'(k_2)} - \frac{K(k_1)}{K'(k_1)} \tag{5}$$

$$d_3 = \frac{K(k_3)}{K'(k_3)} - \frac{K(k_2)}{K'(k_2)} - \frac{K(k_1)}{K'(k_1)} \tag{6}$$

$$d_n = \frac{K(k_n)}{K'(k_n)} - \frac{K(k_n-1)}{K'(k_n-1)} - ... - \frac{K(k_1)}{K'(k_1)} \tag{7}$$

Generally, k_n is defined as [25]:

$$k_n = \frac{1}{cosh(\frac{w\pi}{h_n+h_{n-1}+...+h_1})} \text{ for n=1, 2, 3,...} \tag{8}$$

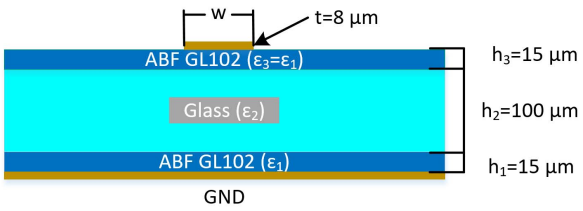
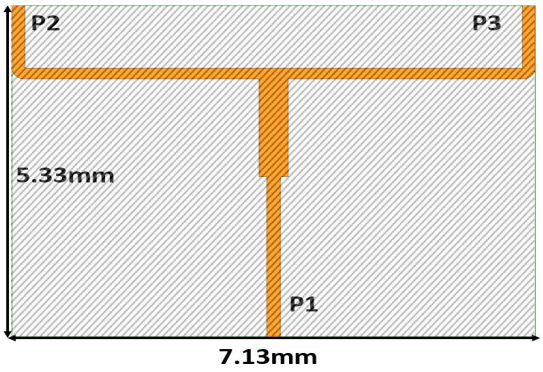
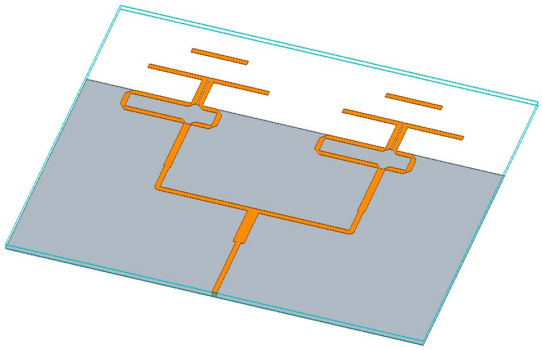


Figure 4. Multilayered microstrip line for power dividers



(a)



(b)

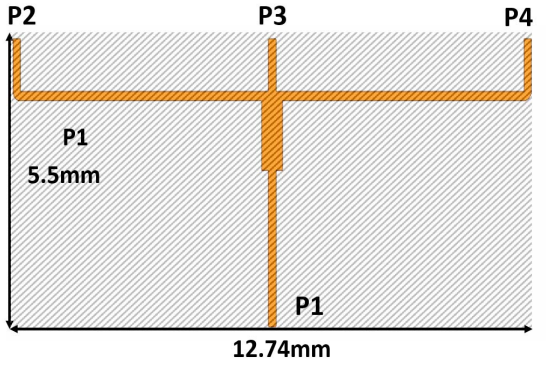
Figure 5. A two-way power divider with a matching quarter-wave transformer (a) simulation layout, and (b) configured as 2×1 antenna array

The value of $\frac{K()}{K'()}$ is given by (9).

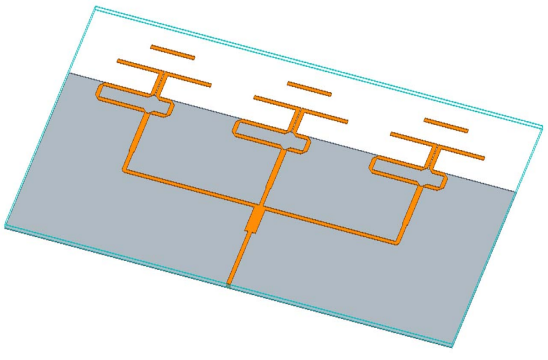
$$\frac{K(k_n)}{K'(k_n)} = \frac{1}{\pi} ln(2\frac{1+\sqrt{k_n}}{1-\sqrt{k_n}}) \text{ for } 0.7 \leq k_n \leq 1 \qquad (9)$$

The frequency-independent relative dielectric constant of the multilayer substrate is obtained using (3)-(9). After obtaining this parameter, the next objective is to find the frequency-dependent behavior of the material stackup. The concept transforms to a single substrate with permittivity ε_{rc} and thickness of $h=h_n+h_{n-1}+...+h_1$ and it is discussed in detail in [26], [27]. It is assumed in this model that the total substrate thickness is approximately equal to $\lambda_0/10$ to obtain quasi-TEM characteristics.

Although calculating frequency-dependent behavior of the multilayer stackup is not absolutely critical below 100 GHz, the frequency-independent ε_{rc} is important as it helps in calculating the width of transmission line corresponding to the characteristic impedance of 50 Ω. The frequency-dependent behavior of the multilayer stackup is useful in accurately finding the electrical length associated with the physical length of the transmission line. Moreover, ε_{rc} can also be estimated intuitively by looking at the contribution of each dielectric to the stackup based on the thickness of individual layer. In this specific case, the ε_1 and ε_3 both equal to Dk of ABF GL102 which makes 30-μm of the total stackup height. The remaining 100-μm is the Dk of glass substrate. Using this data, the Dk of the entire stackup can be estimated to be slightly less than the Dk of glass substrate. Utilizing this technique, width of the microstrip transmission line corresponding to the characteristic impedance of 50 Ω is calculated.



(a)



(b)

Figure 6. A three-way power divider with a matching quarter-wave transformer (a) simulation layout, and (b) configured as 3×1 antenna array

Using this method, the two- and three-way power dividers are simulated. They are also configured as 2×1 and 3×1 using Yagi-Uda antennas which cover the entire 28 GHz 5G band. The layout of both power dividers along with corresponding antenna arrays is shown in Fig 5 and Fig 6, respectively.

III. Fabrication Process of Power Dividers

The fabrication process uses the semi-additive patterning (SAP) process to pattern polymers. SAP enables the fabrication of sub-5 micron features for glass substrates due to their surface planarity and dimensional stability. The process is illustrated with cross-sections in Fig. 7. Proper handling procedures are advised to administer glass fabrication process to address its fragility and brittleness [28], [29]. Polymer lamination on glass addresses the challenge of glass handling and acts a buffer layer that reduces the effect of high CTE copper on glass. It also enables metallization as well as prevents copper migration to glass surface under high electrical voltage during plating.

Through-Glass Vias (TGVs) of 100-μm diameter are drilled by AGC. The glass panels are treated with silane to promote adhesion to polymers and mitigate delamination during the whole fabrication process. Polymer lamination is performed on both sides of glass panel using a roll laminator and 15-μm ABF GL102. This step is followed by polymer curing. The fabrication process continues to via-in-via ablation. The power, power density and number of repetitions are optimized for the UV laser to drill vias in the polymer. This step is performed on both sides of the panel. Next, a 0.2-μm copper seed layer is deposited uniformly on the polymer using electroless plating method. The electroless plating method has a surface roughening step utilizing a permanganate etch which creates mechanical anchor sites on the polymer to enable latching of copper particles. It also helps in removal of residual polymer left after via-in-via ablation.

Afterwards, both sides of the panel are laminated with a 15-μm dry-film negative photoresist. The panel is photolithographically patterned with optimized dose time for the most critical feature of the design. Followed by photoresist development, the panel is subjected to O_2 plasma which removes photoresist residue and improves the surface conditions for copper plating. The metallization of traces and vias is performed using electrolytic plating. SAP yields better dimensions and sidewall control of the deposited copper unlike subtractive etching techniques which have limited control. The target copper thickness after fabrication process is 8-μm so the authors strive to achieve plated copper thickness of 8.2-μm to account for removal of copper seed layer. After electrolytic plating, the photoresist is stripped off using a stripper solvent and seed layer etching is performed. The measured copper thickness

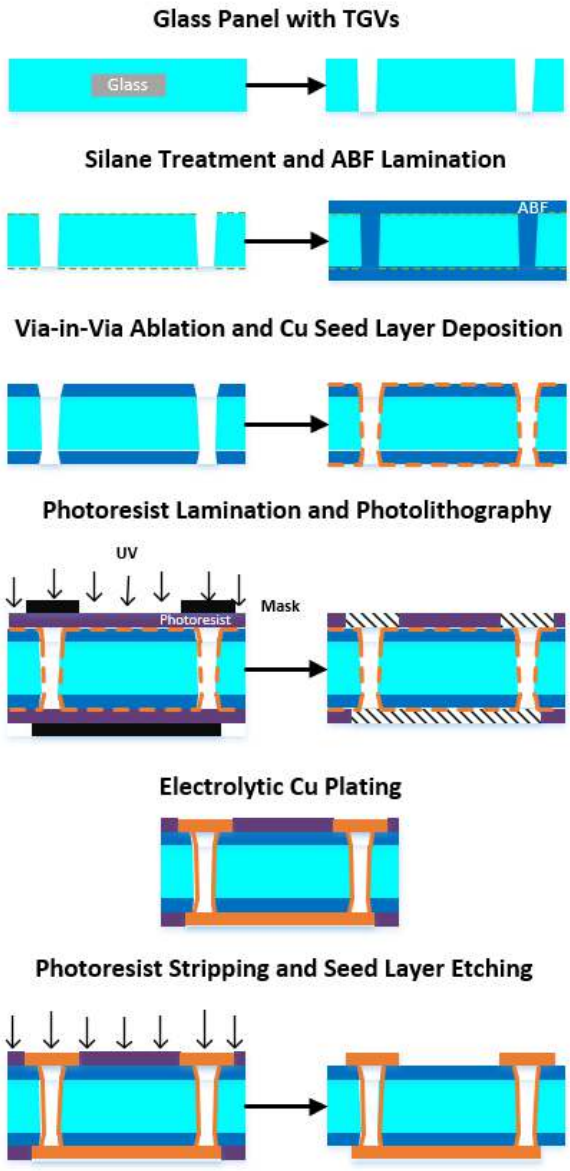


Figure 7. Cross-sectional illustration of SAP

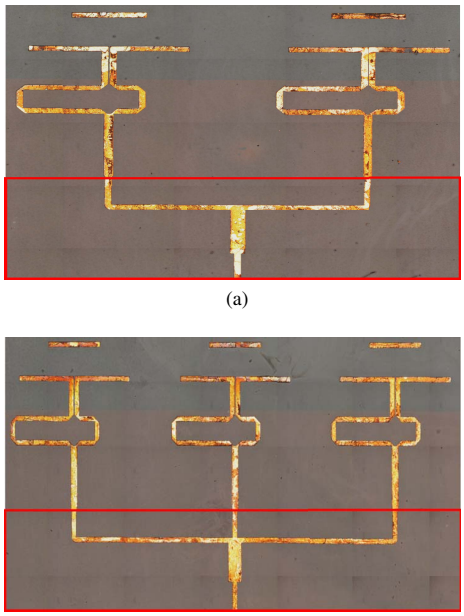
after fabrication process is 8.5±0.5-μm. The fabricated two- and three-way power dividers and antenna arrays are shown in Fig. 8a and Fig. 8b, respectively.

IV. Characterization Results and Analysis

In this section, the characterization results of fabricated power dividers are discussed in detail. The measurements are performed using a VNA in the frequency range of 20-32 GHz using ACP50 GSG probes and Short-Open-Load-Through (SOLT) calibration. For the normalized antenna radiation pattern measurements, the panels are diced into individual coupons and 2.92 mm SMA connectors are soldered onto each coupon as shown in Fig. 9. The measurement results are compared with simulation results to perform a model-to-hardware correlation study. Moreover, dimensional analysis is performed to analyze the fabricated dimensions and compare them with the dimensions in simulation.

A. Two-Way Power Divider

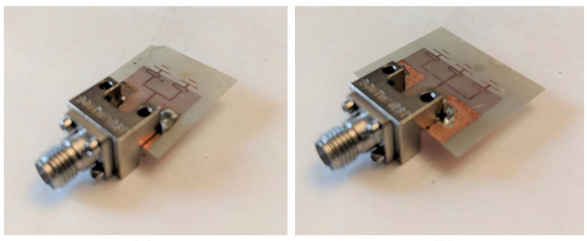
The s-parameters of fabricated two-way power divider are shown in Fig 10. The ideal insertion loss of a two-way power divider is 3.01-dB. As evident from Fig. 10, the power divider has return loss less than 15-dB in the entire 28 GHz 5G band and the insertion loss is fairly constant (∼3.46-dB) as well. The added insertion loss of the two-way power divider is 0.45-dB. Comparison of simulated and measured return loss of 2×1 Yagi-Uda antenna array is shown in Fig. 11. The 10-dB return loss bandwidth of antenna array ranges from 24.3 to 31.4 GHz (FBW=25.5%). The simulated and measured radiation patterns of the antenna array are compared in Fig. 12. It is to be noted that the individual element realized gain of Yagi-Uda antenna



(a)

(b)

Figure 8. Fabricated power divider with Yagi-Uda antennas (a) two-way, and (b) three-way



(a) (b)

Figure 9. Antenna arrays with SMA connectors

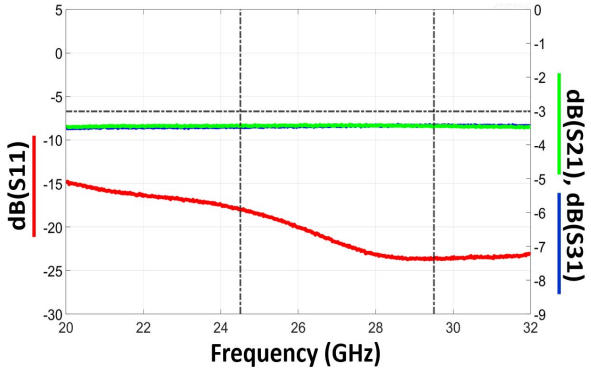


Figure 10. S-parameters of the fabricated two-way power divider

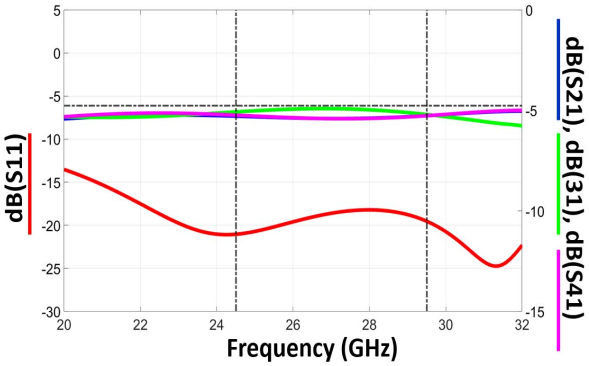


Figure 13. S-parameters of the fabricated three-way power divider

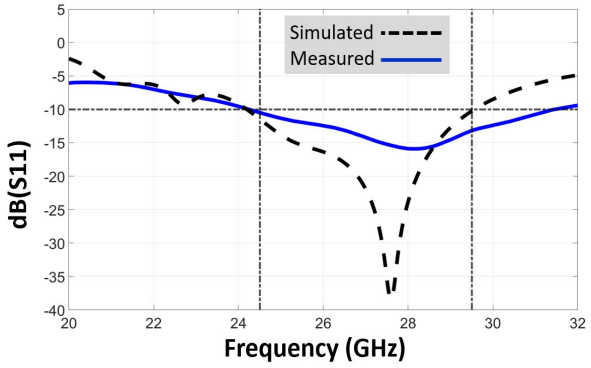


Figure 11. Comparison of simulated and measured S11 of the fabricated 2×1 Yagi-Uda antenna array

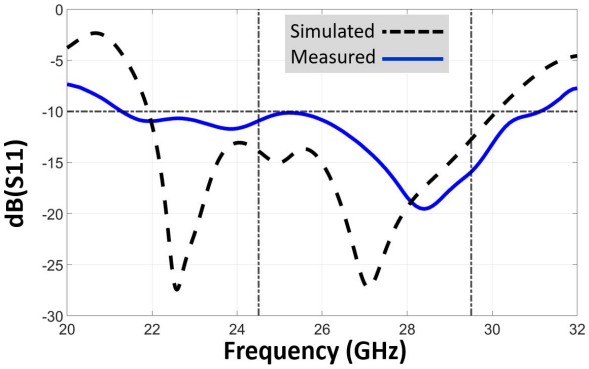


Figure 14. Comparison of simulated and measured S11 of the fabricated 3×1 Yagi-Uda antenna array

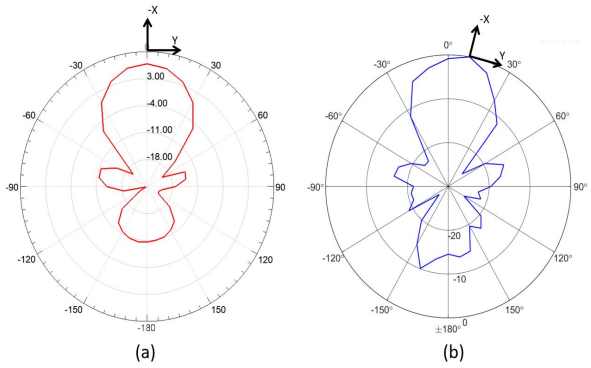


Figure 12. Comparison of simulated and measured radiation pattern of 2×1 Yagi-Uda antenna array

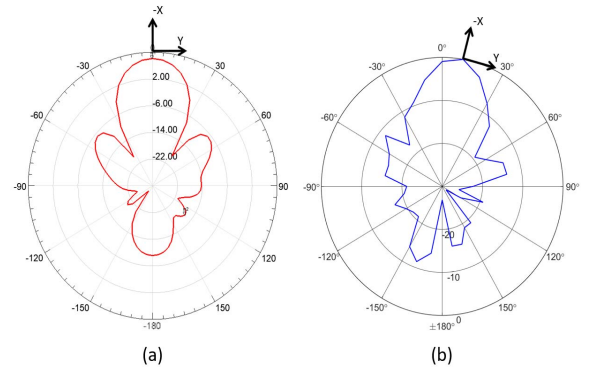


Figure 15. Comparison of simulated and measured radiation pattern of 3×1 Yagi-Uda antenna array

is 4-dB. When configured as a 2×1 array, the realized gain increases to 7-dB with >78% radiation efficiency.

B. Three-Way Power Divider

The s-parameters of the fabricated three-way power divider are shown in Fig 13. The ideal insertion loss of a three-way power divider is 4.77-dB. As depicted in Fig. 13, the power divider has return loss less than 15-dB and a maximum insertion loss 5.42-dB in the entire 28 GHz 5G band. This gives the added insertion loss of the three-way power divider to be 0.65-dB. Comparison of simulated and measured return loss of 3×1 Yagi-Uda antenna array is shown in Fig. 14. The 10-dB return loss bandwidth of antenna array ranges from 21.3 to 31.1 GHz (FBW=37.4%). The simulated and measured radiation patterns of the antenna array are compared in Fig. 15. The realized gain of the 3×1 Yagi-Uda antenna array is 8.24-dB with >85% radiation efficiency.

TABLE I. PHYSICAL AND ELECTRICAL DIMENSIONS OF FABRICATED POWER DIVIDERS AND ANTENNA ARRAYS

Structure	Physical Dimensions (mm^2)	Electrical Dimensions $(\lambda_0)^2$
2-Way Power Divider	5.44×7.13	0.51×0.67
2×1 Antenna Array	14.95×12.33	1.39×1.15
3-Way Power Divider	5.5×12.74	0.51×1.19
3×1 Antenna Array	12.5×20.6	1.17×1.92

C. Dimensional Analysis

The physical dimensions along with the corresponding electrical dimensions in terms of λ_0 of each fabricated power divider and corresponding antenna array is given in Table I. The physical dimensions of the power dividers are normalized by the corresponding free-space wavelength of 28 GHz 5G band: 10.71 mm.

To the best understanding of the author, the fabricated two-way power divider is one of the smallest in terms of x-y dimensions as well as z-height. The total height of the demonstrated power dividers is 147-μm. Moreover, they depict superior performance in terms of low-added insertion loss and minimal phase-shift between the output ports.

V. CONCLUSIONS

This paper presents the detailed design, fabrication and analysis of 3D glass package-integrated, equal-split power dividers with footprint smaller than the unit free-space wavelength corresponding to the operating frequency of 28 GHz 5G band. The power dividers are fabricated using SAP process to meet the dimensional accuracy requirement for such structures on ultra-thin glass. The demonstrated power dividers are also configured as antenna arrays and they can be used in the top metal layers of RF front-end packages where size in all dimensions is a critical requirement The power dividers exhibit low added insertion loss and minimal phase-shift between output ports, making them ideal for strict-footprint 5G and mm-wave module specifications.

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