2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

Low-Loss Additively-Deposited Ultra-Short Copper-Paste Interconnections in 3D Antenna-Integrated Packages for 5G and IoT Applications

Atom O. Watanabe[1], Yiteng Wang[1], Nobuo Ogura[2], P. Markondeya Raj[1,3],
Vanessa Smet[1], Manos M. Tentzeris[1], and Rao R. Tummala[1].
[1]3D Systems Packaging Research Center, Georgia Institute of Technology, Atlanta, GA USA.
[2]Nagase & Co., LTD., Tokyo, Japan.
[3]Florida International University, Miami, FL USA.

***Abstract*— High-bandwidth 5G and 6G communication systems will inevitably migrate to 3D package architectures with backside or embedded dies and antenna-integrated packages for ultra-low losses and smaller footprints. With the trend to such 3D millimeter-wave (mm-wave) packages, the losses from the assembly and through-vias tend to dominate the overall losses. Traditional wirebond and thick solder interconnections lead to large mm-wave interconnect losses that are not acceptable for emerging 5G and 6G communications. This paper focuses on the material syntheses and process development of nanocopper interconnections with ultra-low interconnect losses for chip-last or flip-chip assembly in packages. The first part of the paper introduces the material synthesis of an innovative copper paste with shorter sintering times and temperatures. Optimized conditions are obtained to attain a conductivity of 1.4×10^7 S/m. This is equivalent to 82% increase in conductivity compared to that of solder. The surface roughness is also measured through atomic-force microscopy. Results suggest that the copper paste features higher roughness than that of solders. The second part of this paper discusses the potential of novel nanocopper paste to replace solders as a package assembly material, focusing on the effect of the conductivity and surface roughness with regard to the insertion loss in interconnection bumps. Based on the improved material properties of nanocopper paste, the model shows a 53% reduction in the dB scale at 28 GHz, by employing nanocopper paste. Die shear test for copper paste is also performed to show a high potential to replace solders as a flip-chip assembly material in both printed-circuit-board and mm-wave packaging technologies.**

Index Terms*— *5G communications, Millimeter wave, Low loss interconnect, Interconnect bump, Copper paste, Antenna in package.

I. INTRODUCTION

Ongoing changes in the way humans interact with and consume data is anticipated to create an explosive growth in the number of devices connected to each other as well as to the internet. The bandwidth in electronic communications and wireless sensing in automotive safety, intelligent navigation, wireless sensing and terahertz (THz) communication, and smartphone-like infotainment, communication data rates are projected to be at least 10-100X higher than existing 4G LTE connections [1], [2]. With emerging 5G and 6G communications, trillions of devices with hundreds of radios per person are projected, leading to THz communications with 100 Gbps of bandwidth. In order to realize such systems, heterogeneous active devices and passive components need to communicate within the package and with the outside world in a seamless manner. This trend demands innovative assembly materials or interconnection methods to enable such applications. Conventional methodologies employ wire bonding to form interconnections between the chips and package substrate. However, wire bonds entail more difficult designs in higher frequencies in both IC (e.g., a switch and low-noise amplifier) and package designs because of the increasing parasitic inductance, which causes higher noise figure due to more discontinuity in signal paths and degrades the overall performance. Additionally, wire-bonding methods require more space for landing pads, which makes the miniaturization of IC packages more difficult. Flip-chip technology using solder paste, copper pillar interconnections [3], and all copper [4] addresses the challenges with short interconnection lengths and smaller parasitic inductance [5]. Fan-out packaging is emerging as an alternative approach but flip-chip on low-loss laminate still prevails as the mainstream approach [6] to realize 5G and 6G modules because of its design, material, and process flexibility and simplicity, as shown in Figure 1.

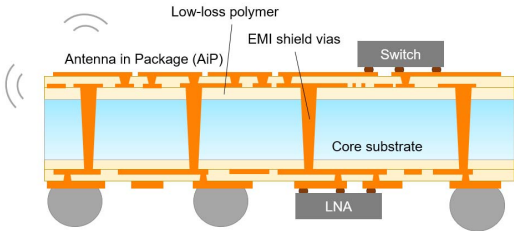

Fig. 1. Antenna-integrated packages with mm-wave chips assembled.

Because of the relatively-low conductivity of solder and process complexity associated with planarization and surface smoothness requirements of direct copper-to-copper interconnections, copper paste is emerging [7], [8] as an ideal material candidate in high-frequency low-loss interconnection assembly. Copper paste shows higher conductivity than solder, given oxidation of copper particles is prevented. The viscosity of copper paste also enables various assembly

2377-5726/19/$31.00 ©2019 IEEE
DOI 10.1109/ECTC.2019.00152

methods such as stencil printing and pin transfer. However, copper paste has not been investigated as a chip-assembly material for 5G or millimeter-wave (mm-wave) applications..

This paper discusses the potential of copper paste as an off-chip interconnection material for high-frequency applications such as 5G and mm-wave communications and RADAR systems. Section II introduces the significance of highly-conductive materials through electrical simulations of flip-chip interconnect bumps between a chip and package. Section III discusses the materials syntheses of various copper pastes, evaluating electrical conductivity, the size of copper particles, and surface roughness, optimizing the sintering conditions. In order to quantify the signal losses caused by interconnect bumps with the synthesized materials, Section IV focuses on the potential of copper paste using fabricated test vehicles with the synthesized materials.

II. MODELING AND DESIGN OF C4 BUMPS EMPLOYED FOR CHIP ASSEMBLY

The objective of this task is to quantify signal losses in interconnect bumps in the frequency bands mainly used for mobile and radar communications. High-frequency signals were designed, as illustrated in the inset of Figure 2. The signal travels from the chip to the package-integrated antenna arrays, through the 50-Ω conductor-backed coplanar waveguide (CPWG) and landing pads. The diameter of the bumps is designed to be 100 μm. In the 3D full-wave electromagnetic (EM) simulation, it is assumed that three frequency bands were chosen and the conductivity of the interconnect bumps was swept from 7.69×10^6 S/m (lead-free solder: SAC305 [9]) through 5.81×10^7 S/m (bulk copper) for twenty bumps in a chain. The signal losses were plotted in Figure 2, implying that high conductivity leads to lower signal losses in interconnect bumps because of the lower signal attenuation and lower heat generation. The results also show that the signal losses at higher frequencies (i.e., 28 and 60 GHz) are more critical than those in the lower frequencies (i.e., 2.4 GHz). Therefore, higher conductivity is essentially required to reduce signal losses and noise figure from the electrical standpoint. The reduction in signal losses lowers the link budget and allows design flexibility in other elements in mm-wave antenna-in-packages.

III. MATERIAL SYNTHESIS OF COPPER PASTE

Higher conductivity with copper paste makes it a compelling alternative to solder in the form of Sn/Ag/Cu (SAC) [9]. However, the major challenge with copper paste is the oxidation occurring on surface of copper particles during the sintering process. This section discusses the design of copper paste interconnections to obtain high conductivity and smooth surface to lower insertion losses in interconnection bumps.

Copper paste (A) with large copper particles with diameters of approximately 1 μm was chosen. After sintering the copper paste A, the electrical conductivity was measured using the four-point probe method, also known as Kelvin method. The copper paste A was annealed at sintering

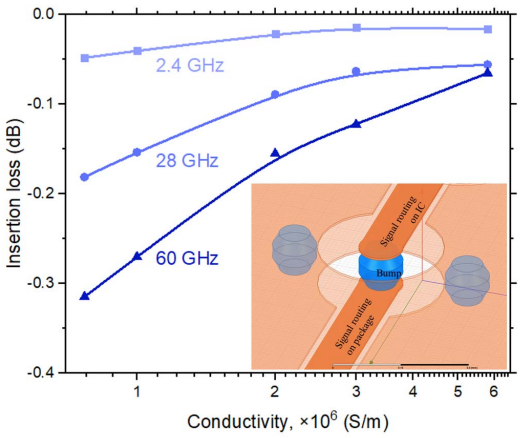

Fig. 2. Insertion loss in interconnect bumps at widely-used frequency bands for RF and 5G/mm-wave applications.

temperatures, T_s, of 200°C and 230°C for half an hour to evaluate the conductivity. Figure 3 depicts the scanning-electron-microscope (SEM) images of the annealed copper paste A at the different temperatures. It is observed in the SEM images that copper particles are not fused with adequate neck formation, which resulted in low conductivity, as listed in Table I. The conductivities under the sintering temperatures were lower than that of solder in the form of SAC305.

TABLE I
MEASURED CONDUCTIVITY OF THE COPPER PASTE A AT TWO SINTERING TEMPERATURES.

	Sintering temperature		
	200°C	230°C	260°C
Conductivity (S/m)	2.14×10^6	3.41×10^6	5.90×10^6

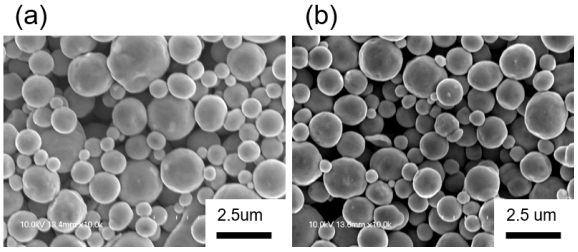

Fig. 3. SEM images of the copper paste A after sintering for 30 minutes at (a) 200°C and (b) 230°C.

To obtain higher conductivity than solder, another copper paste was selected; this copper paste B is bimodal paste, where large and small copper particles coexist and promote high green density in addition to an organic reducing agent. The reducing agent prevents copper from oxidation below 100°C and decomposes at around 100°C. It also reduces the viscosity of copper paste and enables various assembly methodologies such as pin transfer. Sintering under nitro-

gen also prevents copper particles from oxidation. For the optimization of sintering conditions, two parameters (i.e., time t_s and temperature T_s) were varied. To evaluate the copper paste B sintered under each condition, electrical conductivity was measured through the four-point probe method. The results are summarized in Figure 4, comparing to the conductivity of solder in the form of SAC305. The results indicate that the sintering temperature is more critical to the conductivity than the sintering time. The copper paste sintered at 260°C showed higher conductivity than the solder (7.69×10^6 S/m) regardless of the sintering time. The copper paste B sintered for 30 minutes at 260°C showed a conductivity of 1.4×10^7 S/m, which is 82% higher than that of solder. It is found that, controlling the sintered temperature is more significant than the time, implying that the reduction of sintering time with higher sintering temperatures will decrease the time of the total process of chip assembly.

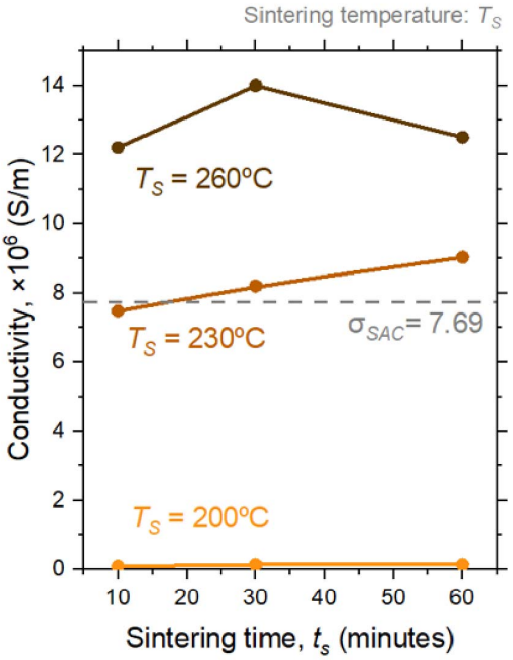

Fig. 4. Measured conductivity of the copper paste B with various sintering time and temperature annealed in the nitrogen gas.

Since the increase in the sintering temperature provided a remarkable improvement of conductivity, we also observed the necking of the copper paste B at each sintering temperatures (200°C, 230°C, 260°C) through SEM. The SEM pictures, as illustrated in Figure 5, show that copper particles at 230°C and 260°C have more interparticle neck formation than the one sintered at 200°C. Copper nano-particle necking is especially observed in Figure 5 (c). Compared to Figure 3, the areas of copper particles sintering are much higher in the copper paste B (Figure 5).

Signal losses are attributed to the ratio of the surface roughness (Δ) to the skin depth (δ). As the surface roughness has a negative impact on the signal loss, the surface

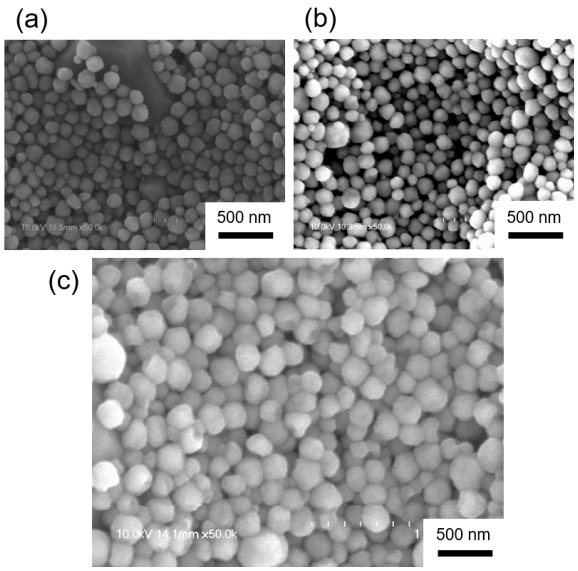

Fig. 5. SEM images of the copper paste B sintered for 30 minutes at (a) 200°C, (b) 230°C, and (c) 260°C.

roughness analysis was performed through atomic-force-microscope (AFM), which provides a very high resolution on the order of fractions of nanometer, more than 10^3 times better than the optical diffraction limit. The roughness causes the conductor loss. Liang *et. al.* [10] identified a good agreement between the attenuation factor between a conductor loss (α_c) and surface roughness (Δ) with a positive correlation in the form of $1+\frac{2}{\pi}\arctan\left[1.4\left(\frac{\Delta}{\delta}\right)^2\right]$. The AFM images are illustrated in Figure 6, showing in the roughness average, R_a, of 162 nm and 81 nm for the copper paste B sintered for 30 minutes at 260°C and the re-flowed solder paste, respectively. While the solder paste offers relatively smooth surface due to the melted and re-formed solder, the roughness of the sintered copper paste B is primarily attributed to the copper bimodal particles with the size of roughly 100 nm, as depicted in Figure 5. The impact of these surface roughness is discussed in Section IV.

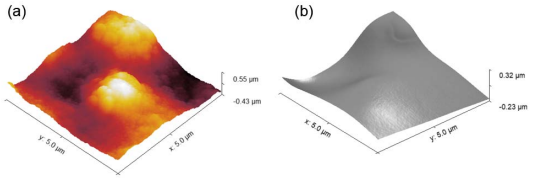

Fig. 6. AFM images of (a) the copper paste B sintered for 30 minutes at 260°C and (b) a reflowed solder paste.

IV. CHARACTERIZATION OF COPPER PASTE FOR CHIP ASSEMBLY

This section discusses the demonstration of chip-last flip chip assembly using the copper paste B. To verify the

potential as the chip assembly material, die shear test is also performed for reliability.

A. Die assembly with copper paste

The daisy-chain structure with a test-chip, utilized in the simulation depicted in the inset of Figure 2, was also employed as the test vehicle. The test vehicles are fabricated through the semi-additive patterning (SAP) process, which provides sub-10μm patterning. The fabricated test vehicles, shown in Figure 7, consist of conductor-backed coplanar waveguides (CPWG) with a spacing of 15 μm and landing pads with a diameter of 100 μm.

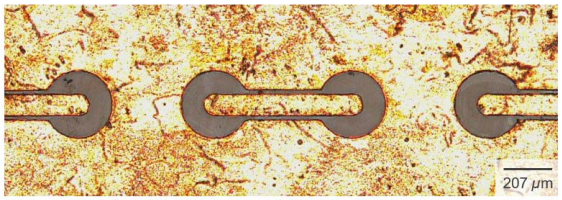

Fig. 7. Top view of the fabricated test vehicle with CPWG and landing pads for flip-chip assembly.

The fabricated test vehicles are assembled through the pin-transfer method, where the copper paste B is transferred from a diameter-controlled pin (80 μm) onto 100-μm landing pads, as illustrated in Figure 8. Once copper paste is provided onto landing pads on the fabricated package, the test-chip is assembled, aligned with the landing pads of both the package and die. This assembly was performed with a pick-and-place assembly machine with an accuracy below 5 μm. The pair of the package and die was annealed under the optimized condition (t_s=30 minutes and T_s = 260°C) discussed in Section III.

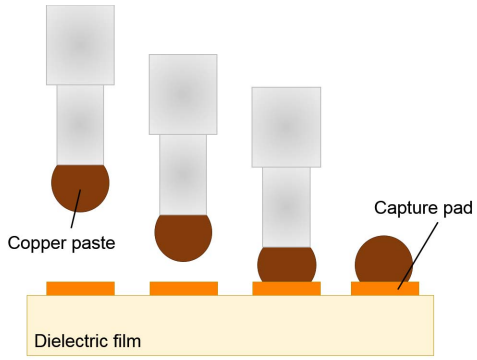

Fig. 8. Pin transfer assembly with a 80- pin for transferring copper paste onto 100-μm landing pads.

The cross-sectional images of the assembled test vehicle at two different locations are shown in Figure 9. The copper paste is observed to deposit within the 100-μm copper pads with diameters of approximately 90 μm. The height of the copper-paste interconnects (4–6 μm) is much shorter than other conventional methods such as C4 and C2 bumps. These shorter interconnects will suppress the parasitic inductance and unwanted electromagnetic interference occurring in bumps. In addition, the accuracy of copper-paste interconnect size is enabled by the control of the amount of copper paste deposited during the pin transfer (Figure 8).

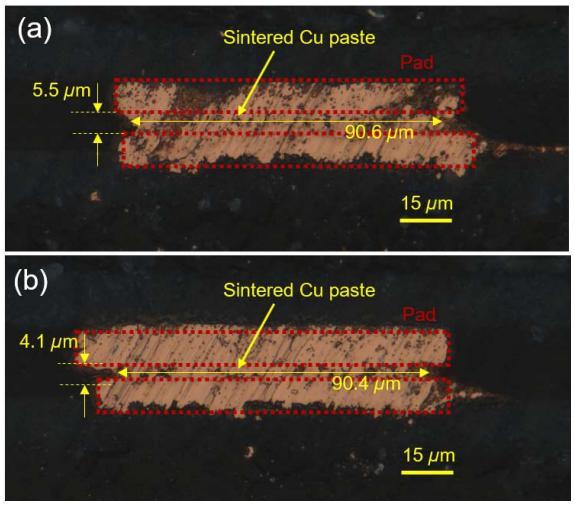

Fig. 9. Cross sectional images through optical microscope at two different locations of the assembled test vehicle with the copper paste B sandwiched by 100-μm copper landing pads.

To quantify the insertion losses in the bumps with the copper paste, the fabricated test vehicle, which includes twenty bumps in a chain, was modeled in the 3D full-wave EM simulator (HFSS). In these simulations, the measured conductivity and surface roughness (Section III) were considered. To verify the chip assembly performance using copper paste, the signal loss when employing solder-paste was also computed. The simulations, summarized in Figure 10, showed an insertion loss of -0.118 dB with copper paste at 28 GHz while the use of solder paste led to an insertion loss of -0.181 dB. Although copper paste features higher surface roughness, this result indicates that the improvement of conductivity reduced signal losses by 53% by employing nanocopper paste.

B. Die Shear Test for Reliability

As an interconnection assembly material in packages, reliability is one of the most significant parameters. Reliability is assessed through a die-shear test, which determines the strength of the system component assembly when subjected to force. A controlled amount of the copper paste B was deposited with pressure, onto a gold surface-finished silicon die, so that the copper paste forms a 6-mm bump shape. A force was applied in the transverse direction using a tensile strength tester, and the material failure occurred at 6.24 MPa before the separation of copper paste from the gold deposited silicon die, as shown in Figure 11. Dark-color circles are the sintered copper paste after the die shear test. This result demonstrates the strong adhesion between the copper paste and gold.

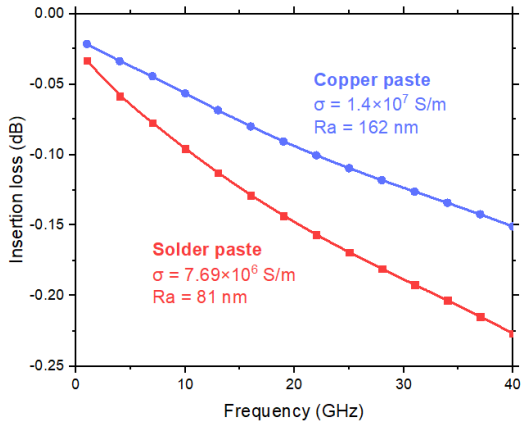

Fig. 10. Insertion loss as a function of frequency, computing the measured conductivity and surface roughness of the copper pate B and solder paste in the form for SAC305.

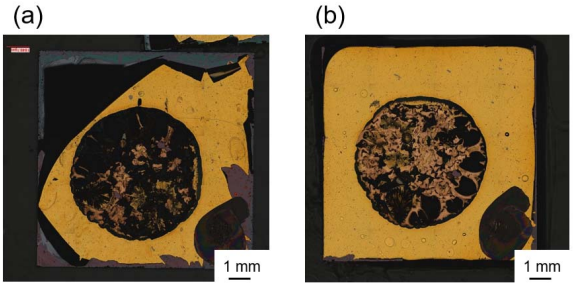

Fig. 11. Microscope pictures of (a) the top die and (b) the bottom die. The black circles

V. CONCLUSIONS

There is increasing need for low-loss ultra-wideband interconnects in the 5G and 6G mm-wave frequency bands to attain seamless chip-to-antenna transitions. This paper focuses on the modeling, material syntheses and process development of off-chip nanocopper interconnections as an alternative to solders. The benefits in conductivity, interconnection height and equivalent surface roughness resulted in a lower insertion loss in the chip-to-package interconnections compared to solder. The first part of the paper discussed the material synthesis of copper paste, optimizing the sintering time and temperature. The optimized conditions with the current nanocopper paste were found with a sintering temperature of 260°C for 30 minutes, which led to a conductivity of 1.4×10^7 S/m. This is equivalent to 82% increase in conductivity compared to that of solder in the form of SAC305. The surface roughness was also measured through atomic-force microscopy. The copper paste showed twice higher roughness than that of solder. The second part of this paper focuses on the potential of copper paste to replace solder as a package assembly material. Computing the material properties of copper paste and solder, the model showed a 53% reduction in the dB scale, at 28 GHz, by employing copper paste. Mechanical reliability was also assessed through a die-shear test. Copper paste was shown to have a high potential to replace solder as a flip-chip assembly material in printed-circuit-board and packaging technologies.

REFERENCES

[1] A. Rashidian, S. Jafarlou, A. Tomkins, K. Law, M. Tazlauanu, and K. Hayashi, "Compact 60 ghz phased-array antennas with enhanced radiation properties in flip-chip bga packages," *IEEE Transactions on Antennas and Propagation*, 2018.

[2] A. Watanabe, T. Lin, P. M. Raj, V. Sundaram, M. M. Tentzeris, R. R. Tummala, and T. Ogawa, "Leading-edge and ultra-thin 3d glass-polymer 5g modules with seamless antenna-to-transceiver signal transmissions," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, May 2018, pp. 2026–2031.

[3] I. Panchenko, M. Kunz, J. M. Mathias Boettcher, L. Lehmann, T. Atanasova, and M. Wieland, "In-line metrology for cu pillar applications in interposer based packages for 2.5 d integration," 2017.

[4] K. Mohan, N. Shahane, R. Sosa, S. Khan, P. M. Raj, A. Antoniou, V. Smet, and R. Tummala, "Demonstration of patternable all-cu compliant interconnections with enhanced manufacturability in chip-to-substrate applications," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, May 2018, pp. 301–307.

[5] N. Li, Y. Wu, L. Chen, B. Wu, C. Zhao, Y. Wang, and Y. Sun, "A novel bump-cpw-bump structure for interconnection/transition of rf mems packaging," in *Electronic Packaging Technology (ICEPT), 2015 16th International Conference on*. IEEE, 2015, pp. 845–847.

[6] L. Del Carro, M. Kossatz, L. Schnackenberg, M. Fettke, I. Clark, and T. Brunschwiler, "Laser sintering of dip-based all-copper interconnects," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*. IEEE, 2018, pp. 279–286.

[7] A. A. Zinn, R. M. Stoltenberg, J. Chang, Y.-L. Tseng, S. M. Clark, and D. A. Cullen, "A novel nanocopper-based advanced packaging material," in *Electronics Packaging Technology Conference (EPTC), 2016 IEEE 18th*. IEEE, 2016, pp. 1–6.

[8] Y. Kamikoriyama, H. Imamura, A. Muramatsu, and K. Kanie, "Ambient aqueous-phase synthesis of copper nanoparticles and nanopastes with low-temperature sintering and ultra-high bonding abilities," *Scientific reports*, vol. 9, 2019.

[9] S. Nai, J. Wei, and M. Gupta, "Effect of carbon nanotubes on the shear strength and electrical resistivity of a lead-free solder," *Journal of Electronic Materials*, vol. 37, no. 4, pp. 515–522, Apr 2008.

[10] T. Liang, S. Hall, H. Heck, and G. Brist, "A practical method for modeling pcb transmission lines with conductor surface roughness and wideband dielectric properties," in *2006 IEEE MTT-S International Microwave Symposium Digest*. IEEE, 2006, pp. 1780–1783.