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A Multi-Channel, Embedded, and Geometrically Optimized Filter Bank Utilizing Advanced Packaging Topologies for Miniaturized RF Modules in IoT and Wearable Systems

Hani Al Jamal Marvin Joshi Manos M. Tentzeris
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, USA
hani.aljamal@ieee.org

Nickolas Kingsley
RF Enabling Technology
Teradyne, Inc.
North Reading, USA
nick.kingsley@teradyne.com

***Abstract*—This paper presents a multi-channel miniaturized RF filter bank by employing advanced packaging techniques such as geometrical optimization, strategic element positioning, and vertical 3D stacking to achieve increased functional density and reduced footprint in RF Printed-Circuit-Board (PCB) modules. Multi-layer PCBs are utilized and RF via structures are designed for showcasing vertically stacked band-pass filters and a 4-channel low-pass filter bank with cut-off frequencies ranging between 7.2 GHz and 16.5 GHz. The resulting filter bank occupying the size of nearly a single integrated circuit (IC) switch not only allows for a remarkable 3X reduction in area, but also reduces cost and manufacturing complexity, allows for easy scalability to 5G/B5G bands and additional channels, and paves the way for flexible/conformal electronics by reducing the number surface mount technology (SMT) components. Furthermore, measurement results demonstrate effectiveness in terms of minimizing signal interference and crosstalk, in addition to achieving superior performance compared to SMT filters. Finally, this paper serves to provide an overview on the design of low-pass and band-pass RF filters.**

***Index Terms*—Filter Bank, Multi-Layer, Printed Circuit Board (PCB), Band-Pass Filter, Low-Pass Filter, RFIC Switch, Via, System-in-Package (SiP), Integration**

I. Introduction

With the ever-increasing demand for smart, wearable, and portable communication devices and systems, miniaturized RF modules with increased functional packaging density, maximum electromagnetic isolation, and reduced footprint have become essential. Advanced packaging approaches allow for the possibility to significantly reduce microwave circuitry while preventing performance degradation or increased production cost. Shrinking circuits by using conventional methods, such as reducing the spacing between components, can cause leakage and crosstalk issues. Throughout literature, a variety of options have been shown to prevent these issues and allow for advanced multi-layer packaging solutions. This includes structures such as staggered and strategically positioned via arrays [1], optimal shape, IC encapsulation and cavity shape modification, field compensating and filtering structures, and AMC/FSS surfaces and resonator elements [2].

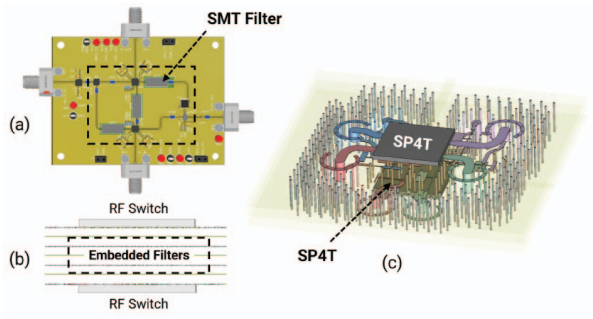

Fig. 1. 4-Channel filter bank implementations. (a) SMT filter bank section on a conventional single-layer PCB consuming a large footprint. (b), (c) Proposed embedded filter bank with a total footprint of nearly the size of one single-pole-four-throw (SP4T) RF switch.

In addition to increased functional density and compactness, miniaturization has a multitude of advantages particularly important in portable and wearable systems for health monitoring, IoT, and AR/VR applications. Miniaturized and Printed Circuit Board (PCB)-embedded filters eliminate the need for surface mount technology (SMT) discrete filters, reducing component and assembly cost, and integrate the filters within the PCB fabrication process, reducing assembly complexity. In addition, SMT components are not suitable for flexible substrates as bending can lead to mechanical failure such as the breakage of solder joints. Furthermore, this approach enhances performance by minimizing signal interference, leakage, and crosstalk issues, and allows for efficient scaling to accommodate additional channels and emerging high-frequency applications. While typical stripline filters are designed in a planar structure, a more compact implementation is achieved in this work by carefully meandering and strategically optimizing the geometry of the filters. In addition, by vertically stacking and

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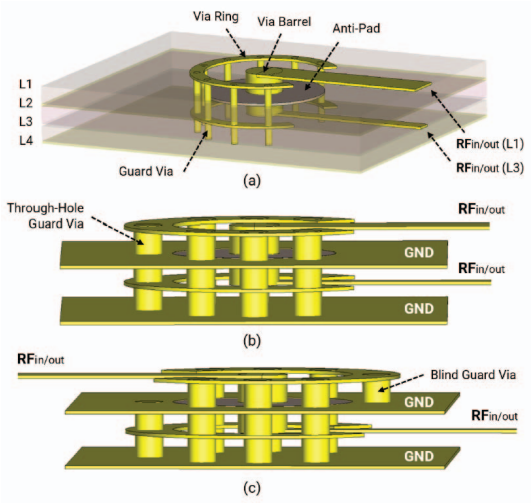

Fig. 2. (a) Via anatomy for RF applications. Side view of a via with (a) 180-degree turn, and (b) 0-degree turn. For illustration purposes, only copper layers are shown.

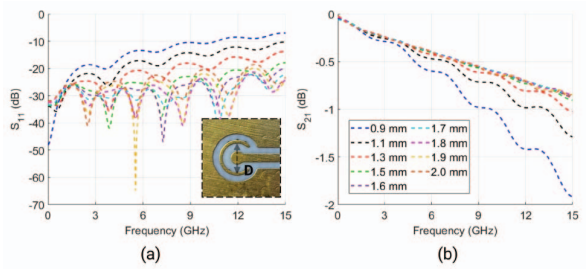

Fig. 3. Simulated reflection and transmission coefficients across a parametric sweep of the via ring diameter (a 180-degree turn via is used). A fabricated via with $D = 1.7$ mm is shown.

embedding the filters in the intermediate layers of the PCB, the overall footprint on the top and bottom layers are reduced as they are only occupied by RF vias that connect the embedded filters to the components on the outer PCB layers. Additional IC components can then make use of this gained board area on both sides of the PCB by "sandwiching" the embedded filters.

This paper explores the use of multi-layer PCBs for miniaturized/embedded RF filter banks. A multi-layer feed-through via structure supporting RF signals is designed and optimized in section II. Then, the design and measurement of two embedded and vertically stacked band-pass filters (BPF) is carried out in section III. Finally in section IV, a 4-channel low-pass filter (LPF) bank with integrated RF switches is geometrically optimized, embedded, and stacked for the highest level of miniaturization and compactness. Fig. 1 illustrates the motivation behind this work showing the PCB footprint reduction from utilizing the proposed embedded/stacked filter bank as opposed to discrete or distributed-element filters on a single layer. The ability to vertically stack filters essentially reduces the filter bank size to the size of just one filter. For a proof-of-concept design, the cutoff frequencies of the four low-pass filters are designed at 7.2 GHz, 11.1 GHz, 13.1 GHz, and 16.5 GHz. The proposed stackable filter bank topology however allows this work to easily be scaled to support additional channels and to be extended for systems operating in 5G/B5G frequency bands.

II. Multi-Layer RF Printed Circuit Boards & Vias

A multi-layer printed-circuit-board (PCB) stackup typically comprises of copper layers, dielectric cores, and laminates impregnated with uncured epoxy resin, known as prepreg, that facilitates the adhesion of two adjacent layers. Understanding the limitations presented by the manufacturing processes used and careful consideration of material selection and layer bonding techniques is paramount to ensuring the manufacturability of miniaturized circuit features within these structures. In addition, vertical transitions from one layer to another can introduce signal integrity issues at high frequencies, such as reflections, impedance mismatch, electromagnetic interference, mode conversion, and insertion loss. Consequently, multilayer PCBs are generally avoided for high-frequency applications.

To design an embedded filter bank effectively, the inclusion of vias (Vertical Interconnect Access) is essential to establish connections between filters situated in intermediate PCB layers and outer layers. However, the transition introduced by these vias can disrupt the clear current path due to the change in reference planes, thereby allowing electromagnetic energy to radiate and excite modes between these planes, ultimately leading to increased insertion loss.

One approach to mitigate this challenge involves the strategic placement of stitching vias around the signal via barrel, which connects to all ground layers within the PCB stackup. These stitching vias serve to provide a closer return current path and effectively direct electromagnetic energy. Positioned around a via ring of diameter D, as depicted in Fig. 2(a), these stitching vias effectively transform the mode of transmission from microstrip or stripline to coaxial.

Furthermore, depending on the arrangement of input/output transmission lines, adjustments to the stitching vias may be necessary, transitioning from through-hole vias to blind vias to prevent overlap between the via and transmission lines. Through-hole vias connect outermost layers, while blind vias connect an outer layer to an inner layer and are are more costly to fabricate. Fig. 2(b) and Fig. 2(c) illustrate two configurations: a 180-degree and 0-degree turn, demonstrating the nuanced considerations in via placement.

As such, the meticulous design of vias at RF frequencies is crucial for ensuring signal integrity. Simulations conducted using CST Microwave Studio revealed insights into the optimal parameters. Specifically, while the diameter of signal and guard vias (via hole) had negligible effects on performance, a minimum wall thickness of five skin-depths is required for low-loss applications. The number and spacing of stitching guard vias directly impact shielding effectiveness and via resonance, but diminishing returns were observed beyond six vias, agreeing with the findings of [5]. Generally, stitching vias

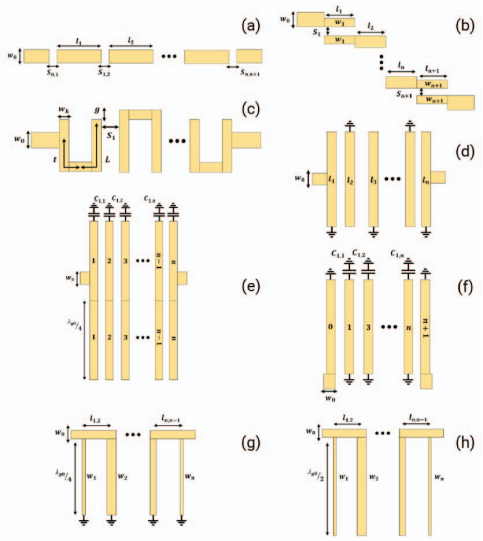

Fig. 4. Band-pass filter distributed-element realizations using transmission lines. (a) End-coupled. (b) Parallel (edge)-coupled. (c) Hairpin. (d) Interdigital. (e) Psedocombline. (f) Combline. (g) Band-pass filter using quarter-wavelength short-circuited stubs. (h) Band-pass filter using half-wavelength open-circuited stubs.

TABLE I
BAND-PASS FILTER DESIGN PARAMETERS

Parameter (mm)	**BPF** ($f_c = 6$ GHz)	**BPF** ($f_c = 12$ GHz)
W_0	0.21	0.21
W_h	0.28	0.18
L	6.74	3.26
t	3.07	1.48
g	0.28	0.18
s_1, s_4	0.058	0.058
s_2, s_3	0.1	0.082
Size (mm^2)	3.6×6.7	2.4×3.2
Size (λ_0^2)	0.07×0.13	0.10×0.13

should be spaced at a distance given by

$$L = \frac{c}{8f\sqrt{\varepsilon_r}} \tag{1}$$

to confine waves within the via transition, with f being the highest frequency.

The diameter of the stitching via ring emerged as a critical parameter affecting insertion and reflection losses the most, as demonstrated in the parametric sweep depicted in Fig. 3. Notably, a ring diameter of $D = 1.7$ mm yielded optimal performance. Additionally, the impact of increasing the number of layers was found to be marginal, underscoring the robustness of the proposed via structure.

III. VERTICALLY STACKED PCB-EMBEDDED BAND-PASS FILTERS

In this section, the design procedure, fabrication, and measurement of two PCB-embedded and vertically stacked band-pass filters are conducted. To realize a band-pass filter using distributed-element transmission lines (stripline transmission lines for embedded filters), several topologies exist and have been extensively studied throughout the literature.

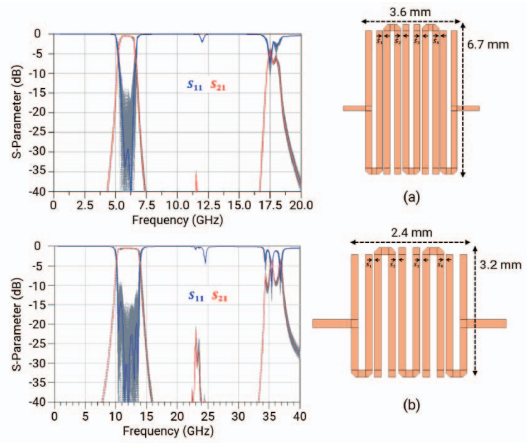

Fig. 5. Simulated performance with tolerance variation on the coupled-line gap width $(s_1 - s_4)$ for the (a) 6 GHz, and (b) 12 GHz 5th order Chebyshev band-pass filters.

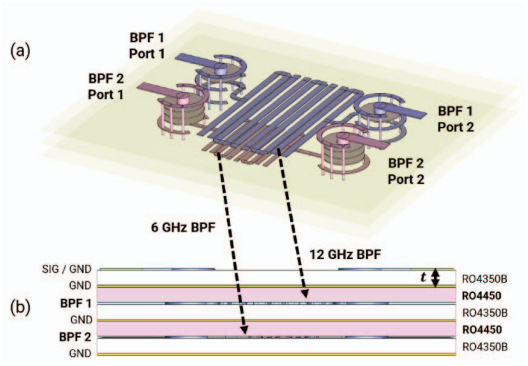

Fig. 6. (a) 3D view and (b) 6−layer stackup of the proposed vertically stacked and embedded band-pass filters.

These include band-pass filter structures such as end-coupled, parallel (edge)-coupled, interdigital, hairpin, combline, pseudocombline, and band-pass implementations using short- or open-circuited stubs, as shown in Fig. 4. For this demonstration, a hairpin filter topology (Fig. 4(c)) is chosen due to its compact footprint. Hairpin filters may be conceptually obtained by folding the resonators of a parallel (edge)-coupled, half-wavelength filter into a U-shape, making the filter smaller in size at the expense of reduced coupling between resonators. The design procedure is detailed in [6], but due to the coupled resonator elements, analytical models serve only as a starting point, and simulation tools such as Keysight ADS should be used.

Two band-pass filters with center frequencies of 6 GHz and 12 GHz are designed, and the optimized design parameters are shown in Table I. Both filters are designed using Chebyshev polynomials of 5th order. Due to the fact that for a given characteristic impedance, stripline transmission lines are narrower than microstrip transmission lines, the embedded hairpin filters are even more compact compared to a microstrip

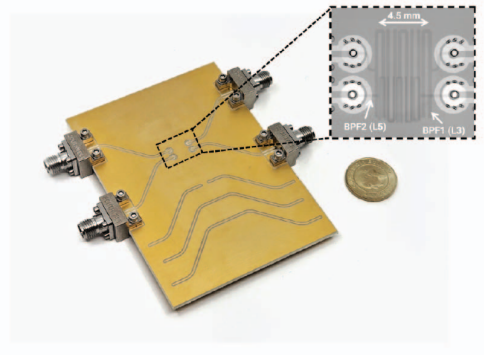

Fig. 7. Fabricated embedded/stacked band-pass filter evaluation board with Southwest End Launch 2.40 mm connectors used. A top view X-ray photograph is shown.

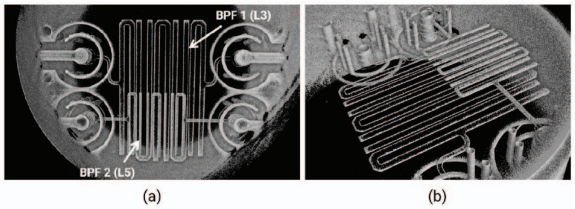

Fig. 8. X-ray photographs of the fabricated embedded/stacked band-pass filters in (a) top, and (b) side views.

realization, with footprints of roughly a tenth of their free-space wavelength. The filter's response is mainly controlled by three parameters: the coupled resonator length (L) affects the resonant (center) frequency, the resonator gap width (s) affects the bandwidth, and the feeding position (t) affects the matching performance. Therefore, certain trade-offs exist between meeting the requirements of wide bandwidth, sharp rejection, and compact size. Moreover, simulations reveal that narrower resonator spacing leads to wider bandwidth. Narrower gaps, however, increase the fabrication cost and complexity.

The stripline band-pass filters are embedded between a core layer from one side (0.254 mm thick Rogers 4350B, $\varepsilon_r = 3.66$, $\tan\delta = 0.0037$), and a prepreg layer from another side (0.284 mm thick Rogers RO4450F, $\varepsilon_r = 3.52$, $\tan\delta = 0.004$). The simulated performance as well as the physical layout of both band-pass filters are shown in Fig. 5. Passbands of $5.2-6.90$ GHz (FBW $= 28.1\%$) and $10.2-13.8$ GHz (FBW $= 30\%$) are achieved. Moreover, due to the fabrication tolerances on the micron-scale resonator gap widths, a sensitivity analysis is performed, changing the gap widths by $\pm 10\%$. The results indicate a robust performance, with S_{11} below -10dB for all width variation combinations across the filters' respective pass-bands.

The designed band-pass filters are then vertically stacked inside a 6-layer PCB stackup on layers 3 and 5, as shown in Fig. 6. Two and four-layer vias are incorporated to connect the embedded filters to the grounded coplanar waveguide (CPWG)

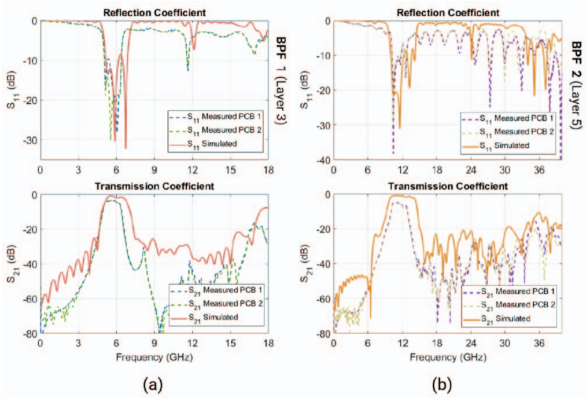

Fig. 9. Simulated and measured S-parameters of the (a) 6 GHz, and (b) 12 GHz band-pass filters. Two boards (PCB 1 and PCB 2) are measured for repeatability.

TABLE II
STACKED/EMBEDDED FILTERS COMPARED TO COMMERCIAL-OFF-THE-SHELF (COTS) SMT EQUIVALENTS

	Embedded Band-Pass Filters	COTS SMT Equivalent)
	Embedded Hairpin ($f_c = 6$ **GHz**)	**BFCN-5750+**
Return Loss (dB)	26.6	19
Insertion Loss (dB)	1.76	2.5
Rejection (dB)	35	25
	Embedded Hairpin ($f_c = 12$ **GHz**)	**BFCN-1262+**
Return Loss (dB)	27.1	11.7
Insertion Loss (dB)	1.12	7
Rejection (dB)	47	45

on the top layer. All other layers are filled with copper and serve as reference ground planes. As aforementioned, a prepreg layer is required to bond two adjacent core layers. In the proposed stackup, alternating layers of Rogers RO4350B (core) and RO4450F (prepreg) are used and considered in simulation. The prepreg layer has a dielectric constant of 3.52, which differs by 0.14 from that of the core layer.

A fabricated proof-of-concept board is shown in Fig. 7. A modified semi-additive process (mSAP) capable of achieving line width/space features of 20μm/20μm is used to fabricate the intricate coupled resonator line width/space of 176μm/58μm. X-ray photographs of the fabricated PCB-embedded and vertically stacked band-pass filters are shown in Fig. 8 depicting how the two stacked filters occupy the size of one.

Two prototypes are measured to ensure repeatability, and the results are plotted against the simulations in Fig. 9 for the two filters. Great agreement between simulation and measurement is shown, with both filters achieving a measured return loss, insertion loss, and rejection of better than 26.6 dB, 1.76 dB, 35 dB, respectively. These results are tabulated in Table II and compared to commercial off-the-shelf (COTS) SMT filter counterparts. In addition to the advantage of embedded filters enabling board miniaturization, the measured filters outperform equivalent COTS SMT filters.

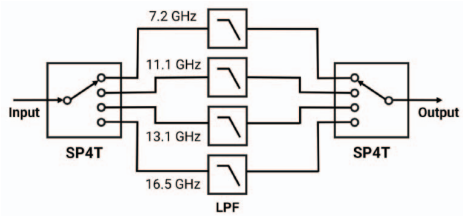

Fig. 10. Block diagram of the proposed 4-channel low-pass filter bank.

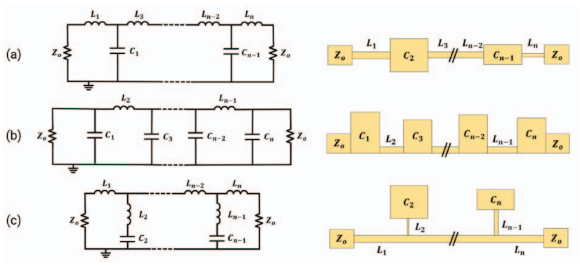

Fig. 11. Low-pass filter types and their corresponding distributed-element realizations using transmission lines. (a) Stepped-impedance L-C ladder-type. (b) L-C ladder type using open-circuited stubs. (c) semi-lumped type with finite-frequency attenuation poles.

IV. 4-Channel Embedded Low-Pass Filter Bank

In this section, a compact 4-channel low-pass filter bank utilizing meandered stripline filters is designed. The block diagram of the filter bank, as shown in Fig. 10, comprises two single-pole-four-throw (SP4T) RF switches and four low-pass filters with operational bands of DC–7.2 GHz, DC–11.1 GHz, DC–13.1 GHz, and DC–16.5 GHz. These filters are embedded within two intermediate layers of a PCB, with two filters situated on each layer. The two switches are then placed on the outer PCB layers (top and bottom) and connected to the embedded filters using the via structures discussed in section II. Consequently, the 4−channel filter bank occupies nearly the size of one switch.

Depending on the low-pass filter response type, several distributed-element realizations exist, as summarized in Fig. 11. For the proof-of-concept demonstration, 7th order elliptical low-pass filters are designed. While elliptical filters (transfer functions) exhibit ripple in both the pass- and stop-bands, they offer the steepest roll-off compared to maximally-flat Chebyshev transfer functions. An elliptical transfer function is derived from the lumped-element filter of Fig. 11(c) with its corresponding transmission line implementation shown. This implementation utilizes shunt capacitors as low-impedance (wide) transmission lines and series inductors as high-impedance (narrow) transmission lines. The design of a distributed-element low-pass filter is outlined in detail in [3] and [4]. The procedure involves selecting an appropriate low-pass response type (such as elliptic, Chebyshev, Butterworth, or Bessel) and order number based on the desired pass- and stop-band requirements. Lumped L-C elements are then derived based on tabulated "g-values" and the desired cut-off frequency. Finally, the lumped elements are transformed into a transmission line realization approximating the lumped-element filter.

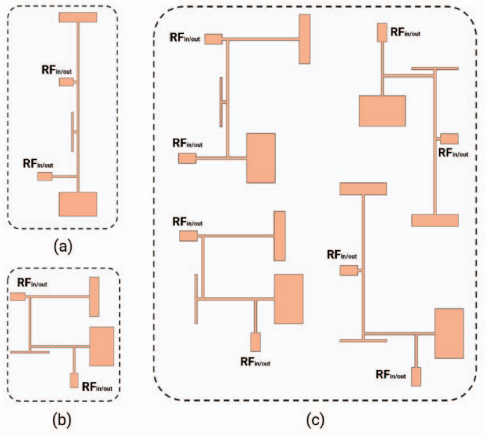

Fig. 12. Geometric optimization of a 7th order elliptical low-pass filter (cut-off frequency $f_c = 11.1$ GHz) for optimal board space utilization. (a) Direct implementation (total length is 6 mm). (b) Meandered design. (c) Other possible geometric configurations of the same filter.

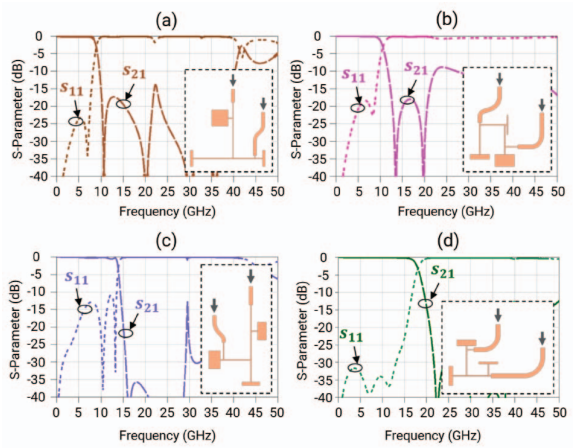

Fig. 13. Simulated performance and layout of the four semi-lumped type meandered low-pass filters with cutoff frequencies of (a) 7.2 GHz, (b) 11.1 GHz. (c) 13.1 GHz, and (d) 16.5 GHz. Note that the arrows in the layout represent an input/output port.

The semi-lumped implementation of one such filter with a cut-off frequency of 11.1 GHz is shown in Fig. 12(a). This direct implementation, however, does not facilitate miniaturization nor integration with other filters on the same layer and/or vertically stacked filters on other intermediate PCB layers. To utilize the minimum footprint on a single layer, the filter geometry must be geometrically optimized in regard to other filters on the same layer. At the same time, vias connecting those filters to the outer PCB layers are strategically placed to consume the smallest footprint on the outer PCB layers. Therefore, a co-design optimization strategy must be considered to optimize the layout of the filters through creative

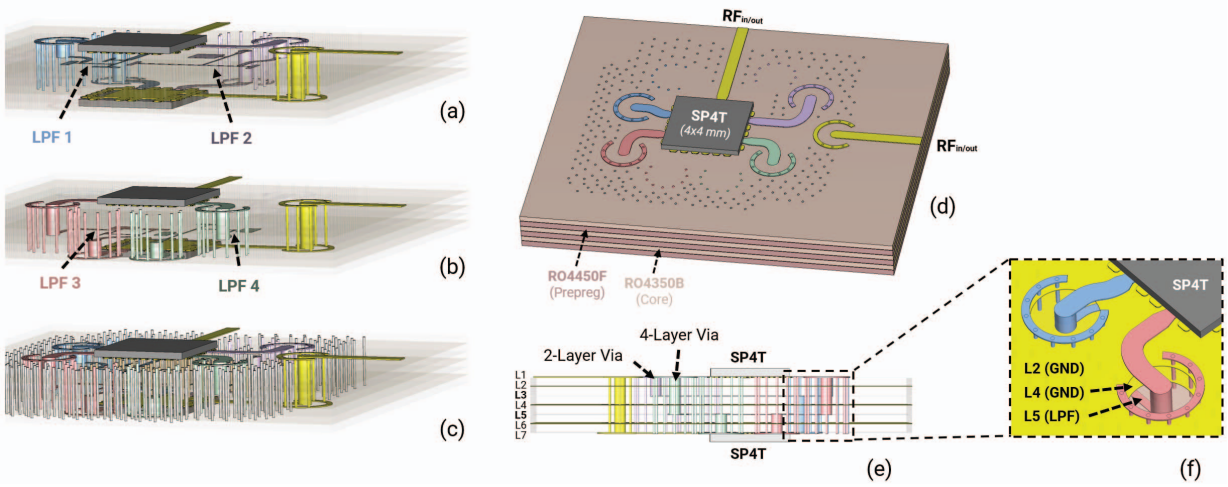

Fig. 14. 3D view of the designed 4-channel low-pass filter bank highlighting (a) two meandered filters on layer 3, (b) two meandered filters on layer 5, and (c) via shielding and stitching. PCB stackup in (d) top, and (e) side views. (f) RF via connecting the top switch to a filter on layer 5 using a 4−layer via.

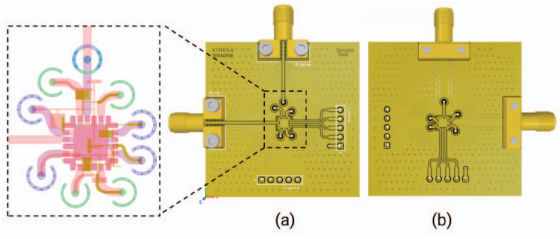

Fig. 15. Low-pass filter bank proof-of-concept PCB. (a) Top view showing multi-layer 2D layout. (b) Bottom view. Purple colored vias connect a transmission line on the top layer to a filter in an intermediate layer, while green colored vias connect a transmission line on the bottom layer to an intermediate layer filter.

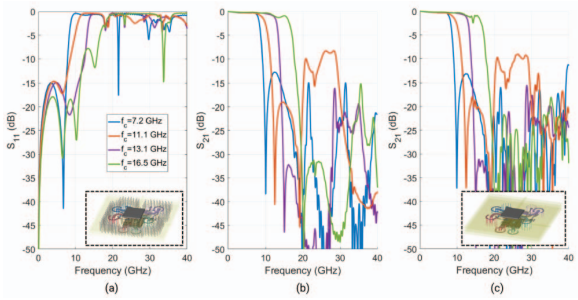

Fig. 16. (a) Reflection, and (b) transmission coefficients of the proposed filter bank. (c) Transmission coefficient with no via shielding/stitching used.

meandered geometries taking via placement and other filters in the PCB stackup into account. As will be evident later in this section, as the number of channels/embedded filters (and RF vias) increases, the complexity of the optimization problem increases exponentially given the increased number of constraints.

The four low-pass filters are strategically meandered using Keysight ADS for optimal performance and minimal footprint. Filters with cut-off frequencies of 7.2 GHz and 16.5 GHz are placed on one intermediate PCB layer, while filters with cut-off frequencies of 11.1 GHz and 13.1 GHz are placed on another intermediate layer. Fig. 13 shows the simulated performance and layout of the four filters designed using stripline transmission lines, with the same dielectric stackup as described in section III.

Simultaneously, CST Microwave Studio is utilized to strategically position vias connecting each filter to two SP4T switches on the top and bottom layers while avoiding any copper overlap. Four vias connect the switch on the top layer to the input ports of the embedded filters, while a set of four other vias connect the output ports of the filters to the switch on the bottom layer. Stitching vias, a periodic array of vias, are added across the board to connect ground layers, ensuring shorter ground return paths, and improved signal integrity. The spacing requirement on stitching vias for the purposes of blocking electromagnetic wave propagation is the same as described in section II. Shielding vias are also added along the perimeter of the microstrip lines to provide a low-impedance path for the return current induced along the edge of the stitching vias. The 3-dimensional stackup illustrated in Fig. 14 is comprised of 7 layers, with filters embedded in layer 3 and 5. While an odd number of PCB copper layers is more complex to fabricate due to the increased possibility of warpage during fabrication, ensuring a symmetrical copper distribution (or equivalently total copper area) between layers $1-3$ and $4-7$ facilitates the process.

The ADRF5045 SP4T switches utilized on the top and bottom layers control which filter is in operation from the filter bank. The ADRF5045 is a 4×4 mm non-reflective silicon-based switch with a low insertion loss of 2.4 dB up to 30 GHz. As opposed to reflective-type switches that leave unused ports as unterminated (open or short- circuited), non-reflective-type

switches, also referred to as absorptive, terminate all RF ports in the off-state condition. As a result, these switches offer better return loss and higher isolation, linearity, and power handling capabilities. The switch is controlled through two bias voltages allowing the RF signal to be directed to any of the four ports and achieves switching speeds below 6μs.

A proof-of-concept PCB is designed to demonstrate the performance of the proposed 4-channel miniaturized filter bank (Fig. 15). The filter bank consumes a footprint of 9.2 mm $\times$ 9.8 mm $=$ 90 mm^2 including the two switches and all vias, with the board measuring 1.77 mm thick. Finally, the filter bank's transmission and reflection coefficients simulated using CST are plotted in Fig. 16(a) and Fig. 16(b), respectively. S_{11} is better than -15 dB, and S_{21} is better than 1 dB for all filters across their respective passbands. Plotted in Fig. 16(c) are the transmission coefficients in the absence of any stitching or shielding vias. As evident, the response becomes noisy, especially at higher frequencies.

V. Conclusion

In conclusion, this paper presents a comprehensive exploration of advanced packaging topologies for miniaturized RF modules. By leveraging multi-layer PCBs and strategically embedding filters within, we have demonstrated significant reductions in footprint without compromising performance. The vertically stacked band-pass filters and 4-channel low-pass filter bank showcase the efficacy of our design approach in achieving increased functional density and compactness. Furthermore, simulation and measurement results demonstrate performance enhancements when compared to SMT filters, underscoring their potential for enhancing portable communication devices and systems in IoT and wearable applications. While a low-pass filter bank with 4-channels was presented, the design workflow outlined allows the scalability of additional channels or other filter types and frequency bands. Moving forward, further optimization and integration efforts hold promise for realizing even greater miniaturization and performance improvements in RF filter technology.

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