Inkjet-Printed 3D Interconnects for Millimeter-Wave System-on-Package Solutions

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***Abstract*—This work outlines the development, fabrication, and measurement of fully inkjet-printed 3D interconnects for wireless mm-wave packaging solutions. Conductive silver nanoparticle and dielectric polymer-based inks are utilized to fabricate die attach, dielectric ramp, and CPW transmission line interconnect structures in order to interface a silicon die with a packaging substrate. Insertion and return loss are measured and compared with simulations over the range of 0–40 GHz. An inkjet-printed mm-wave bow-tie slot antenna is integrated with the IC die in order to highlight the highly versatile nature of this 3D interconnect technology for integration with emerging SoP technology.**

***Index Terms*—Interconnects, SoP, inkjet printing, mm-wave packaging, mm-wave antenna.**

I. Introduction

Current trends in emerging wireless technologies are pushing for the realization of high bandwidth data transmission and miniaturized form factor, along with a simultaneous reduction in cost. This next generation of mobile communication systems has taken root in the field of millimeter-wave (mm-wave) wireless technology, where carrier frequencies operate within the range of tens to hundreds of gigahertz. This increase in frequency from typical commercial microwave technologies allows for wider bandwidth channels, establishing interest in such fields as autonomous automotive radar and gigabit local area networks. Because of the reduction of wavelength in the mm-wave regime, packaging technology becomes especially important in the development of any practical system. In order to miniaturize wireless systems and reduce destructive high-frequency parasitics, the realization of system-on-package (SoP) packaging solutions is an area of popular research, where integrated circuit (IC) dies can be integrated directly with peripheral components, such as other ICs, antennas, and various other passive components.

Three-dimensions (3D) first-level interconnects are required in order to interface an IC die with a packaging substrate and other electronic components within the same package. The two most popular methods of realizing these interconnections are wire bonding and flip-chip techniques. Wire bonding is a relatively cheap and rapid interconnection option, yet it is often prone to sway upon molding and high parasitic inductance, often requiring passive components for compensation at mm-wave frequencies [1]. Flip-chip techniques reduce interconnection length and parasitics yet suffer from high sensitivity to coefficient of thermal expansion (CTE) mismatch as well as detuning from the close proximity to on-package signal routing below the IC [2].

In order to assess the current challenges of cost and versatility in wireless mm-wave SoP solutions, this work outlines the development of 3D interconnects using inkjet printing, a rapid, fully additive electronic fabrication technology with the benefits of zero waste, reduced cost, and increased design flexibility. Coplanar waveguide (CPW) transmission lines are fabricated and measured to interconnect a silicon die with a packaging substrate using conductive silver nanoparticle and dielectric polymer inks as a first-of-its-kind proof of concept. These fully printed interconnects are then used to integrate a die with a mm-wave bow-tie slot antenna to demonstrate the feasibility of realizing low cost, robust SoP wireless systems.

II. 3D Interconnect Design

The design of the 3D interconnects is composed of the following elements shown in Fig. 1: an IC die, a packaging substrate, a die attach material, a dielectric ramp structure, and CPW transmission lines. For this work, a blank 2 x 2.7 mm silicon die with a thickness of 50 µm and a bulk resistivity of 10 ohm-cm is used as a proof-of-concept prototype for mm-wave transceiver dies. The packaging substrate is chosen to be a 1 mm thick glass slide in order to facilitate handling throughout the fabrication process, however this technology could be applied to other packaging substrates, such as metallic, flexible organic, and ceramic.

A die-attach material is used to adhere the silicon die to the glass packaging substrate. In order to create a three-dimensional transition between the top of the die and the substrate below, ramp structures are also required to transition the 50 µm thickness of the die. These components are realized with an SU-8 polymer-based dielectric ink, a formulation of 35 w% of the long-chain SU-8 polymer from MicroChem, a cyclopentanone solvent, and a negative UV-cross-linking agent. The dielectric structures patterned with this ink exhibit a thickness of 4–6 µm per printed layer, with a relative permittivity (ϵ_r) of approximately 3.2 and a loss tangent (tan δ) of approximately 0.04 at 24.5 GHz [3], [4].

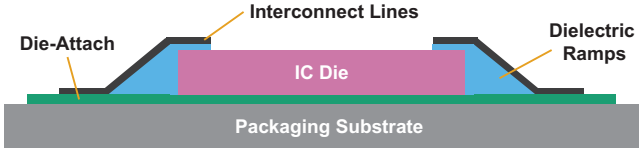

Fig. 1. Cross-section of proposed inkjet-printed 3D interconnects.

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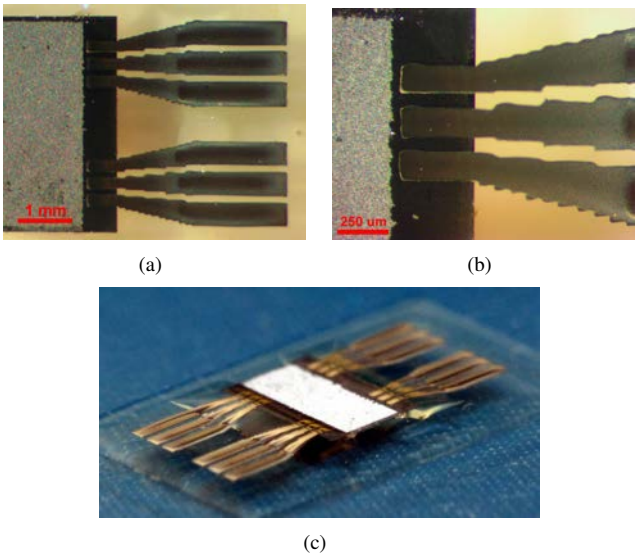

(a) (b)

(c)

Fig. 2. (a–b) Micrographs and (c) perspective image of the inkjet-printed CPW interconnect samples.

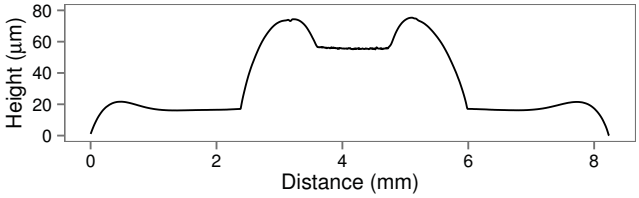

Fig. 3. Profilometer scan of the inkjet-printed 3D interconnect sample, including: die attach, ramp structures, and silicon die.

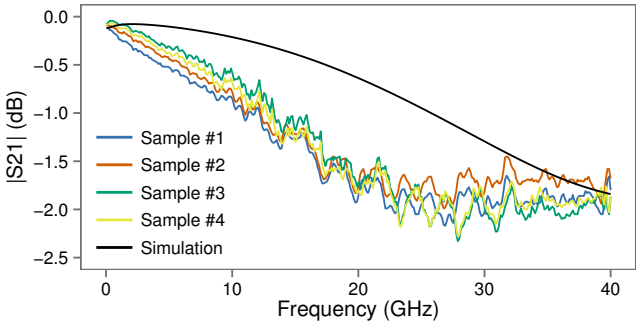

Fig. 4. Insertion loss simulations and measurements for the inkjet-printed first level CPW interconnects.

In order to interconnect the top of the die to the packaging substrate, 50 Ω CPW transmission lines are employed with a fan-out structure to maintain the desired impedance considering the transition of ϵ_r between the die (ϵ_r = 11.9) and the substrate (ϵ_r = 4.82). These conductive patterns are realized with Cabot CCI-300, a silver nanoparticle-based ink utilizing an alcohol-based solution for low-temperature ($<$ 200 °C) processing. After sintering, the printed silver patterns exhibit conductivity in the range of 10^7 S/m [5].

III. Inkjet Printing Fabrication Process

Fabrication of the 3D interconnect samples begins with the patterning of the die attach material on a bare glass slide using a Dimatix DMP-2831 piezoelectric inkjet materials printer. Three layers of the SU-8 polymer ink are printed and then baked with a 60–120 °C ramp over 10 min. A silicon die is then manually placed onto the die attach, followed by the remainder of the SU-8 ink curing profile: a 250 mJ/cm^2 exposure of 365 nm ultraviolet (UV) light and a 100 °C bake for 7 min. For this demonstration, the die attach is acting as an adhesion layer for both the die and the printed interconnects on the packaging substrate.

With the die attached, dielectric ramps are printed to transition between the die and the substrate. The ramp structures are patterned to extend approximately 400 µm onto the surface of the die and 800 µm onto the substrate. The purpose of extending the pattern onto the surface of the die is to allow for a uniform ramp to be realized with the minimum amount of printed layers, where adhesion of the ramp to the top of the die is expedited when material is deposited onto both the the die and the substrate instead of the substrate alone due to the rheological nature of the polymer ink. Additionally, the extension of the material onto the die allows for increased adhesion of the printed interconnects to the unpolished surface of the die. Five layers of the SU-8 polymer ink are printed to pattern the ramps, followed by the previously outlined curing profile with the substitution of a 300 mJ/cm^2 UV light exposure to account for the thicker dielectric ramps.

Fabrication is concluded with the printing of the CPW transmission line traces. Before printing, the sample undergoes a 30 sec exposure to UV ozone (O_3) to optimize the surface energy of the printed ramps and substrate for the wetting of the CCI-300 ink. Three layers of the silver nanoparticle ink are printed, followed by oven sintering at 180 °C for 1 hr.

IV. Inkjet-Printed Interconnect Measurements

Images of the printed 3D CPW interconnect samples are shown in Fig. 2. The staggering effect present in the fan-out of the traces is due to the 20 µm resolution of the CPW line pattern. The key dimensions of the printed CPW interconnects exhibit on average less than ± 3% variation across the four printed samples. A profilometer scan is presented in Fig. 3, detailing the height of the printed die attach, ramp structures, and silicon die. The height of the three-layer die attach is measured to be 16 µm and exhibits good uniformity across the center of the film where the die is placed. The maximum height of the five-layer ramp structures reaches up to 20 µm above the die attach due to the presence of printed material on the surface of the die as well as the natural tendency of the SU-8 polymer ink to form a convex profile when a high density of material is printed in a limited area [3]. The surface of the 50 µm die is measured to be 40 µm above the die attach, determining that the die recesses approximately 10 µm into the die attach under the outlined processing conditions.

High frequency simulations of the CPW interconnect prototypes are conducted using CST Microwave Studio. The S-

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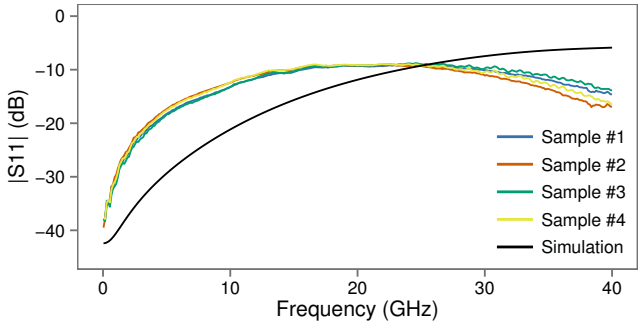


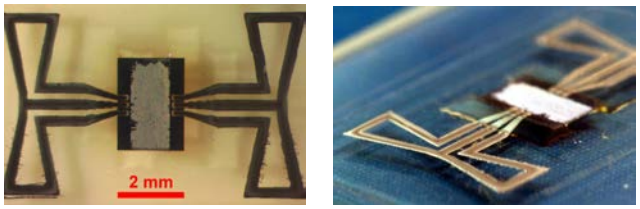
Fig. 5. Return loss simulations and measurements for the inkjet-printed first level CPW interconnects.

parameters of the printed interconnect samples are measured with an Anritsu 37369A VNA utilizing 250 µm pitch ground-signal-ground (GSG) probes from Cascade Microtech. Insertion and return loss parameters include the interaction of three general forms of loss in a standard transmission line: dielectric loss, conductive loss, and radiated loss. Measured and simulated insertion loss parameters from 0.04–40 GHz are presented in Fig. 4. The measured results of the printed samples show excellent consistency with each other, however discrepancies less than 1.5 dB in magnitude are witnessed throughout the band. Deviations from the simulation values are likely the result of the morphology of the dielectric ramp structures, a feature that is difficult to precisely model in simulation. Fig. 5 presents the measured and simulated return loss parameters over the same frequency range. As with the insertion loss measurements, excellent consistency between the printed samples is demonstrated. Deviation from simulated return loss is likely the result of imperfections present in the 3D modeling of the GSG probes used for measurement.

V. On-Package mm-Wave Antenna Integration

In order to demonstrate the effectiveness and versatility of entirely inkjet-printed 3D interconnects as SoP applications, integration with a mm-wave antenna is presented. A bow-tie slot antenna is chosen in order to preserve the efficiency of the CPW feed line interconnect from the die. The bow-tie slot antenna offers a simple planar design along with a wide operational bandwidth suitable for mm-wave wireless technologies. The antenna is designed to operate beyond the 24.5 GHz ISM band using a miniaturized wideband bow-tie slot configuration. This frequency range is also suitable for probe station measurement where the metallic chuck acts as a reflector to antenna on the glass packaging substrate, which has an approximate electrical thickness of $\lambda/4$ around 30 GHz.

The fabrication of the antenna samples is identical to that of the inkjet-printed CPW interconnects previously outlined. Images of the printed mm-wave bow-tie antenna samples that are connected to the IC through the proposed inkjet-printed 3D interconnects are presented in Fig. 6. With the exception of several minor instances of nozzle failure during printing, the printed samples exhibit good consistency with each other and the intended design pattern.



(a) (b)

Fig. 6. (a) Micrograph and (b) perspective image of the inkjet-printed on-package mm-wave bow-tie antenna samples.

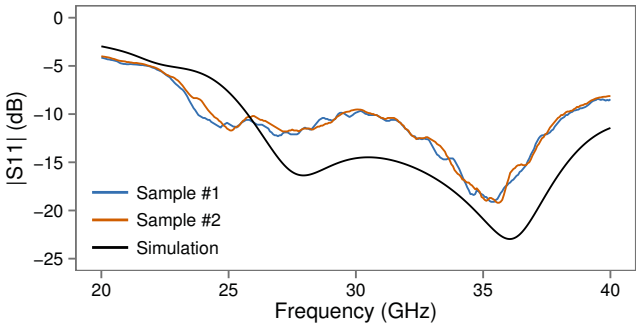


Fig. 7. Return loss simulations and measurements for the printed mm-wave bow-tie slot antennas.

Return loss measurements of the printed antennas are recorded to verify the effectiveness of the presented 3D interconnect method for mm-wave wireless systems. Fig. 7 presents the measured and simulated return loss parameters of the two printed antenna samples over the range of 20–40 GHz. The measured return loss of the printed samples exhibits resonance within and beyond 24.5 GHz ISM band. Deviations from the simulated return loss are likely the result of the presence of the GSG probes used for measurement, as well as the morphology of the SU-8 ramps previously discussed. Farfield simulations of the bow-tie antenna yield a radiation efficiency of 51% and a realized gain of 6.3 dB in the endfire direction away from the die and 1.6 dB in the broadside direction at 30 GHz. Radiation efficiency has the potential to be increased through the investigation of lower-loss dielectric ink formulations for the printed die attach and packaging substrate structures.

VI. Conclusion

For the first time, this work outlines the utilization of fully-additive inkjet printing technology to fabricate 3D mm-wave interconnects. CPW transmission lines are employed to interconnect a silicon die with a packaging substrate, exhibiting suitable insertion and return loss for mm-wave systems. To highlight the robust nature of these printed interconnects, a mm-wave bow-tie slot antenna is integrated with a silicon die in a SoP scenario. The integration of inkjet printing technology with wireless mm-wave packaging technology has the potential to set the foundation of the next-generation of scalable fully-customizable versatile wireless systems well within the mm-wave frequency range.

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ACKNOWLEDGMENT

The authors would like to acknowledge the National Science Foundation (NSF) for their support with this work.

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