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# Flexible and Scalable Additively Manufactured Tile-Based Phased Arrays for Satellite Communication and 5G mmWave Applications

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*Abstract*— **This paper presents a novel flexible and scalable tiled phased array antenna operating in K band, with individual phased array tiles and a corporate feeding network achieved by microstrip-to-microstrip transition. The prototype fabrication utilizes additive manufacturing to achieve low-cost and flexible features. Both simulation and measurements for a 2 by 2 array demonstrate good radiation and beam steerability. The basic structure of this four-tile array can be conveniently scaled to any larger array of $2^N$ elements or for higher frequency applications. This design can be applied to active phased-array radars and support future demand for high volume 5G communication.**

*Keywords*— **additive manufacturing, phased array, satellite communication, 5G.**

## I. INTRODUCTION

The recent development of 5G and mmWave technologies has enabled next-generation Internet of Things (IoT) and massive MIMO systems, with high data-rates and wideband operation. To satisfy the link budget, large antenna arrays are required to support these applications[1]. However, some requirements in fabrication and assembling may limit the total size of the antenna arrays. Especially for satellite communication systems, the power consumption is constrained by battery capacity and traditional large arrays are bulky and heavy and not suitable for small UAVs. Additionally, the designs need to be highly scalable to meet the manufacturability requirements. Typically, these challenges have been studied on a system level to achieve the balance between antenna size and other factors. A simpler solution has been proposed to have a smaller size light-weight antenna array in an integrated tile-based structure, while maintaining high gain and low cost[2]. Most designs in past research have all the tiles integrated with phase control and amplifier circuits in one board[3], which usually requires multilayer stackup or increases the total area of the array. This brings more challenges in fabrication and scalability, along with higher cost and complexity. Additive manufacturing can address these issues by inkjet-printing planar phased arrays onto light weight and flexible substrates and integrate them with beamforming RFIC in a low-cost and efficient manner. It provides the possibility to customize array shape and allows for selective deposition of materials in a 3D fashion to enable vertical integration[4].

This paper presents a highly scalable, compact and lightweight additively manufactured tile-based phased array, including small standalone phased array tiles, and a tiling layer with feeding structure to connect each tile by a novel microstrip-to-microstrip transition. The removable tile elements allow the array to change the dimension based on different requirements. Anokiwave Beamforming IC is utilized on single tile for phase and amplitude control of patch antennas. The inkjet-printed flexible tiling layer also enables the complete phased array to be conformally wrapped around a curved surface such as the wings of a small UAV. These features make the proposed tiled phased array an ideal candidate for space-limited and power efficient 5G and satellite communication applications, and mmW Rx systems for multi-streaming with high throughput that require a large number of antenna arrays[5].

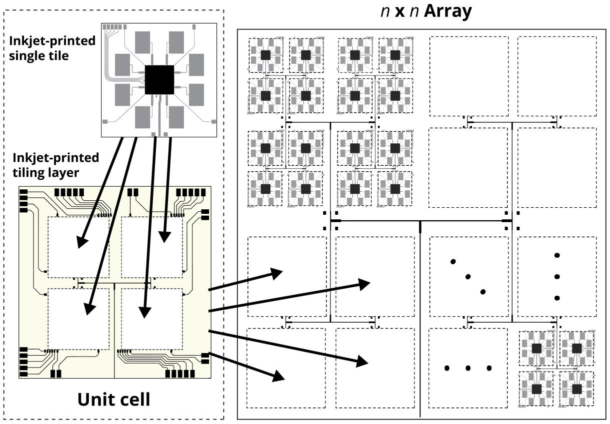

Fig. 1. Scalability demonstration of the tile-based phased array.

## II. TILED PHASED ARRAY DESIGN

### A. Single Tile

The structure of the single tile phased array consists of an Anokiwave Beamforming IC AWS-0102, and 8 microstrip patch antennas. AWS-0102 is a K-band SATCOM Rx Quad Core IC, which supports 8 radiating elements and 17.7-20.2GHz operation. It has integrated phase shifters and SPI communication to control the phase of each element. When more tiles are included in the array, simultaneous multi-chip control can support beam steering of a larger phased array through SPI configuration. As shown in Fig.1, for each single tile, 8 edge-fed patch antennas are connected to the chip by feed lines with impedance matching to 50 Ohm. The patches are faced to opposite direction to save total area of the board and the resulting out-of-phase performance can be compensated in phase control.

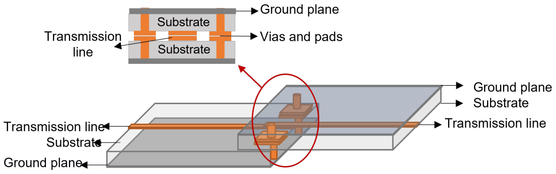

Fig. 2. Microstrip-to-Microstrip transition.

### B. *Tiling Layer Design*

The tiling layer is used to attach the tiles to the feedline and provides connection to outer circuits such as SPI, VCC and ground signal. The design of the tiling layer is shown in Fig. 1. The SPI and VCC signal lines from each tile are further extended as soldering pads on the tiling layer. The feed line connects the RF beam out on each tile to total Rx output. All the ports are matched to 50 Ohm by quater-wavelength transformers. Based on this feeding structure, a 2 by 2 tiled array can be considered as a “unit cell”, and it can be easily extended to larger scale of any $2^N$-tile array by duplication, as shown in the demonstration from Fig. 1. To scale to other frequencies, the only parameter that needs to be adjusted is the dimension of patches and feedlines.

In addition, to attach each tile to the feedline, a novel microstrip to microstrip transition is applied. Fig. 2 shows the GSG transition design between two microstrip lines, as well as a cross-section view of this structure. Two vias are placed aside the transmission line to connect ground planes of tiles and tiling layer. Square pads are added at the top of vias to reduce difficulty in soldering and provide higher stability. It has been reported that this structure can realize a low-loss and wide-band transmission[6].

## III. FABRICATION

The tiling layer was additively manufactured on Rogers 3003 substrate of 0.13mm thickness, with a dielectric constant of 3 and a loss tangent of 0.001. This substrate is flexible and can be bent over curved surfaces. SU8 ink (MicroChem) was first inkjet-printed on the substrate with circuit trace pattern and cured by UV Crosslinker. Then the sample was etched in ferric chloride to remove the copper without SU8 layer. When the etching stops, the tiling layer was cleaned using water and acetone to wash off the residue. Vias for the microstrip-to-microstrip transition were made by drilling 0.2mm holes on the soldering pads, then silver paste (LPKF ProConduct, $\rho = 9.42 \times 10^{-6}\Omega$m) was applied to fill the holes, followed by a sintering at 160°C for 30 min. Finally, the squared holes for placing the single tiles were cut by a milling machine. All inkjet printing was performed using a DMP-2831 printer (Fujifilm Dimatix, Inc.)

For proof of concept, fabricated individual tiles from PCB etching are used in this paper to test the functionality of the proposed tiled phased array. However, individual tiles can also be additively manufactured on flexible substrate. Fig. 3a shows an example of a single tile inkjet-printed on Kapton HN (127$\mu$m thick) using silver-nanoparticle ink (EMD5730, Sun Chemical). Three layers of silver ink were used to ensure good conductivity. The major challenges in additively-manufactured tiled array come from inkjet printing resolution and surface wetting on the substrates. As shown in Fig. 3a, single tile design requires compact routing of SPI signal lines between two neighbouring patches, which is constrained by the footprint of the RFIC. This has been addressed by using a printing cartridge with a drop volume of 1 pl (Dimatix DMC-1160), as well as utilizing only two nozzles at the printing time. Kapton substrate was used in this design because it can remain stable across a wide temperature range (-269 to +400 °C), which is applicable for satellite communication environment. In order to enhance the ink adhesion, the Kapton substrate was pretreated by submerging in a 1 M NaOH solution for 1 hour and then thoroughly rinsed with water. This method has improved the surface wetting to a great extent. Future work will be focused on utilizing inkjet-printed tiles in the design.

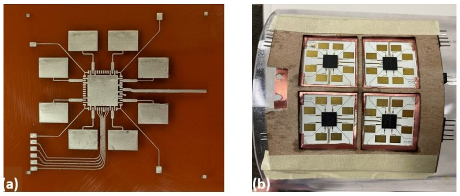

Fig. 3. (a) Single inkjet-printed tile on Kapton; (b) Assembled tiled array bent over a curved surface.

To assemble the full tiled array, solder paste was applied on all the pads of the tiles and tiling layer to work as joints between vias, and each tile was flipped to align the corresponding pads. Then a heat gun was used to reflow the solder on the pads and provide stable connection between separate components. This approach demonstrated to have excellent adhesion for the microstrip-to-microstrip connection. The alignment between the tiles and tiling layer represents a crucial step for the assembly process. One way it can be overcome is to design the soldering pads along the edge of the squared holes, so that the tiles can be placed at precise position. The whole assembly process is similar to soldering a QFN package. Finally, header pins were soldered to the pads of the tiling layer to connect SPI, VCC and ground signals through jumper wires and cables. Sample frame is fixed on the front side of the array to facilitate measurements. The whole structure is very stable once connected and can be easily reproduced in inkjet printing using the same printing pattern. As shown in Fig. 3b, the assembled phased array can be conformally wrapped over a curved surface without any detachment of the tiles.

## IV. SIMULATION AND MEASUREMENT RESULTS

Both single tile and full tiled phased array were simulated in CST Microwave Studio and measured in an anechoic chamber. The dimension of patch and distance between patches have been optimized in simulation for good radiation and low side lobe level during beam steering. The measurement setup

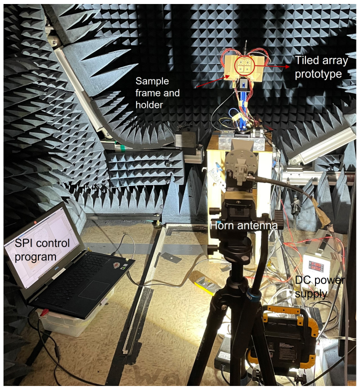

Fig. 4. Measurement setup

is shown in Fig. 4. A sample holder and a sample frame are required to keep the flexible prototype fixed in vertical position.

Figures 5a and 5b show the radiation pattern and beam steering for single and 4 tiles phased array, respectively. The steering angle for both single tile and 4 tiles phased array can reach -50 to 50 degrees. A slight asymmetry is noticed between two steering directions, which can be caused by misalignment between horn antenna and phased array. For the 4-tile array, as the steering angle increases from 0 to 52 degree, the beamwidth increases from 15 to 25 degree. This effect can be improved by applying tapering to reduce amplitude of the patches away from the center of the array. The highest side lobe level (SLL) obtained during the steering measurement was -9.7 dB. The SLL slightly increases in measurements, possibly due to the existence of large amount of cables and a copper ground plane around each tile. This can be further improved by switching to more flexible cables and etching off the unnecessary copper. The main contribution to higher back side lobe in measurements are the cables for SPI connection that were taped behind the sample holder.

The measured and simulated results are overall in good agreement, and the discrepancy is due to the fabrication tolerance and measurement errors. Table 1 compares this work to other state-of-art phased array designs including additively manufactured ones. Shin et al. present a 3D printed polymer-based horn antenna phased array that has very high gain with fewer elements. 3D printing enables a customized structure of the horn antenna integrated with power dividers as feedline[7], but it's bulky and not conformal compared to planar arrays. The inkjet printed phased array on flexible substrate proposed by Subbaraman et al. demonstrates good performance, but the phase shifter circuits largely increase the total area. Overall, this paper introduces the first additively manufactured tile-based phased array that features excellent scalability to very large number of antenna elements up to the 5G/mmW frequency range, low cost, low profile and lightweight, meanwhile can achieve superior performance than similar phased array designs.

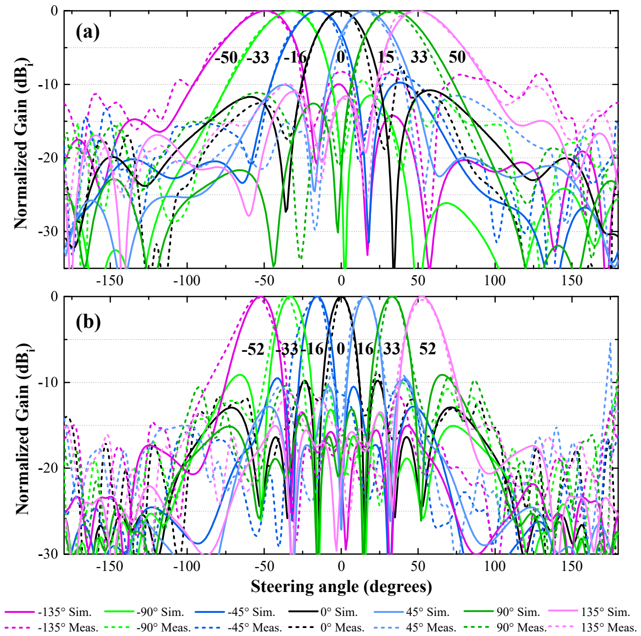

Fig. 5. Simulation and measurement results for a single tile phased array (a) and for the 2×2 tiles ("unit cell") phased array(b).

Table 1. Performance comparison with previous work

| Parameter | This work | [8] | [7] | [9] |
|---|---|---|---|---|
| **Frequency** | 19GHz | 19GHz | 17GHz | 5GHz |
| **Fabrication** | Inkjet Printing | PCB etching | 3D Printing Electroplating | Inkjet Printing |
| **Element** | 32 | 8 | 4 | 16 |
| **Realized gain[dBi]** | 16 | 11 | 17 | 14.6 |
| **SLL[dB]** | -9.7 | -5 | -10 | -11 |
| **Steering angle[degree]** | 50 | 70 | 26.5 | 34 |
| **Area[$mm^2$]** | 56*56 | $\sim 55*110$ | $\sim 50*100$ | 120*120 |
| **Thickness[mm]** | 0.5 | 0.8 | $\sim$ 20 | NA |

## V. CONCLUSION

This work presents a functional, flexible and scalable tile-based phased array operating at 19GHz, using inkjet printing and rugged microstrip-to-microstrip transition. It is the first time that an additively manufactured tile-based phased array is reported. The fabricated 2×2 tile "unit cell" phased array prototype shows good radiation (16dBi gain) and beam steering capability (+/-50 deg steerability) at the center frequency of 19GHz. Based on the results from such "unit cell", a fully inkjet-printed 4×4 tiled phased array (2×2 "unit cells"), including 128 patch antenna elements, will be shown at conference, and it will target a realized gain of 22dBi and a SLL of -11dB. The proposed design of fully additively-manufactured tiles and tiling layer enables the possibility to assemble very large and customizable phased arrays in a rapid and a low-cost fashion, which can be widely used in 5G mmW applications.

## REFERENCES

[1] A. S. Abdellatif, W. Zhai, H. K. Pothula, and M. Repeta, "Array of arrays: Optimizing phased array tiles," *IEEE Antennas and Wireless Propagation Letters*, vol. 20, no. 5, pp. 718–722, 2021.

[2] A. Gupta, U. Madhow, A. Arbabian, and A. Sadri, "Design of large effective apertures for millimeter wave systems using a sparse array of subarrays," *IEEE Transactions on Signal Processing*, vol. 67, no. 24, pp. 6483–6497, 2019.

[3] R. W. Lyon, A. M. Kinghorn, G. D. Morrison, A. Stonehouse, G. Byrne, and M. Dugan, "Active electronically scanned tiled array antenna," in *2013 IEEE International Symposium on Phased Array Systems and Technology*, 2013, pp. 160–164.

[4] B. K. Tehrani, R. A. Bahr, W. Su, B. S. Cook, and M. M. Tentzeris, "E-band characterization of 3d-printed dielectrics for fully-printed millimeter-wave wireless system packaging," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 1756–1759.

[5] A. Ghasemi and S. A. Zekavat, "Low-cost mmwave mimo multi-streaming via bi-clustering, graph coloring, and hybrid beamforming," *IEEE Transactions on Wireless Communications*, vol. 20, no. 7, pp. 4113–4127, 2021.

[6] K. Hu, X. He, and M. M. Tentzeris, "Flexible and scalable additively manufactured antenna array tiles for satellite and 5g applications using a novel rugged microstrip-to-microstrip transition," in *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (APS/URSI)*, 2021, pp. 37–38.

[7] S.-H. Shin, D. F. Alyasiri, M. D'Auria, W. J. Otter, C. W. Myant, D. Stokes, Z. Tian, N. M. Ridler, and S. Lucyszyn, "Polymer-based 3-d printed ku-band steerable phased-array antenna subsystem," *IEEE Access*, vol. 7, pp. 106 662–106 673, 2019.

[8] N. O. Parchin, H. J. Basherlou, and R. A. Abd-Alhameed, "Dielectric-insensitive phased array with improved characteristics for 5g mobile handsets," *Progress in electromagnetics research M Pier M*, vol. 94, pp. 209–219, 2020.

[9] H. Subbaraman, D. T. Pham, X. Xu, M. Y. Chen, A. Hosseini, X. Lu, and R. T. Chen, "Inkjet-printed two-dimensional phased-array antenna on a flexible substrate," *IEEE Antennas and Wireless Propagation Letters*, vol. 12, pp. 170–173, 2013.