RF Tag Front-end Design for Uncompromised Communication and Harvesting

John Kimionis, *Student Member, IEEE*, and Manos M. Tentzeris, *Fellow, IEEE*

***Abstract*—Typically, low-cost and low-power backscatter radio communicators utilize a switching mechanism for alternating the antenna load between two values. In this way, they achieve modulation by reflection of the RF waves induced at the communicator's antenna. For tags that employ a rectifier for wireless energy harvesting, a single transistor may switch between the matched harvester and a reflective load (an open or short). However, optimized backscatter communication occurs when switching between two reflective loads, ideally an open and a short. This prohibits the use of a harvester that requires a good matching (i.e. no reflections) and produces a tradeoff of either compromising communication performance or not employing a harvester. Although this may not pose a problem for commodity RFID tags that operate in short ranges and do not require high computational ability, it is a strong limitation for applications like wireless sensor networks that employ backscatter radio as a low-cost and low-power communication scheme. In this work, an RF front-end is designed, analyzed, and implemented, that overcomes the limitation of compromising communication performance when employing a harvester.**

***Index Terms*—backscatter radio, communication, harvesting, RFID, tag design.**

I. Introduction

For low-power and low-cost wireless connectivity scenarios, backscatter radio may be used to reduce the cost and energy requirements of each communicator's radio frequency (RF) front-end to a fraction of those required by classic active radios. The principles of backscatter radio have been successfully used in commercial radio frequency identification (RFID) applications [1], [2], authentication applications [3], and sensing applications [4]–[8]. Since backscatter radio achieves communication by RF signal reflection rather than active radiation, the signal-to-noise ratio (SNR) of the tag-backscattered (i.e. reflected) signals at the reader is typically small and thus backscatter radio is a short-range communication scheme [9]. The need for optimized communication is very prominent in backscatter radio, since the operating SNR is commonly low; an analysis of the effects of the backscatter channel to the backscatter link performance is given in [10]. The factors that affect the communication performance are analyzed in [11], where directions for improved-communication RF tag design are given. Moreover, in [12], [13] directions for enhanced-range backscatter communication are given, by utilizing non-conventional reader architectures that provide for increased SNR and lower bit-error-rate (BER) at the reader in long-range scenarios.

A binary backscatter modulator consists of an antenna with impedance Z_a which is terminated with a load Z_0 for bit '0' or a load Z_1 for bit '1'. A switching mechanism is needed to alternate the antenna load impedance between the two values Z_0 and Z_1; usually, the switching is achieved by utilizing an RF transistor properly biased to operate at the cutoff or saturation region. When a load Z_i is present at the antenna terminals, the antenna-load reflection coefficient is

$$\Gamma_i = \frac{Z_i - Z_a^*}{Z_i + Z_a}. \tag{1}$$

The constraint associated with BER minimization at the reader is described by [11]:

$$\max|\Delta\Gamma| \triangleq \max|\Gamma_1 - \Gamma_0|, \tag{2}$$

which essentially means that the complex reflection coefficients Γ_1 and Γ_0 should have the maximum possible distance on the Smith Chart of impedances. Also, from [13], where the complete backscatter radio signal model is derived by accounting for both microwave parameters and wireless communication channel parameters, it is straightforward that the tag signal SNR at the reader and the reflection coefficient distance $|\Delta\Gamma|$ are related by:

$$\text{SNR} \triangleq \frac{E_b}{N_0} = \frac{P_{\text{tag}}\, T_b}{N_0} \propto |\Delta\Gamma|^2\, T_b. \tag{3}$$

E_b is the bit energy, P_{tag} is the average power of the received tag signal at the reader, T_b is the bit duration (bit period), and N_0 is the noise power spectral density. In other words, the tag-backscattered signal captured by the reader has energy proportional to $|\Delta\Gamma|^2$ and T_b. One obvious way to increase the received SNR is to increase the bit duration, i.e. lower the tag bitrate $R_b = 1/T_b$. On the other hand, for a given tag bitrate, control over Γ_0, Γ_1 is needed to increase the SNR at the reader by maximizing $|\Delta\Gamma|$.

Ideally, by utilizing the load values $Z_0 = 0$ (short-circuit) and $Z_1 = \infty$ (open-circuit), the two reflection coefficient values are $\Gamma_0 = -1$ and $\Gamma_1 = 1$, respectively, and their distance is $|\Delta\Gamma| = 2$. This is the maximum achievable $|\Delta\Gamma|$ value when utilizing purely passive loads,[1] and thus corresponds to optimally selected Z_i values that will achieve minimum BER at the reader for a given reader transmission power, operating distance, tag antenna gain, and tag bitrate.

There are cases where an RF tag does not have a dedicated power source and is powered up by the reader-transmitted signals (such as in passive RFID tags) or may have some small battery that needs to be periodically recharged by exploiting the reader-transmitted RF power (useful scenario for backscatter-enabled sensor networks). In both cases, a

The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA, 30332-0250. Email: {ikimionis@gatech.edu, etentze@ece.gatech.edu}.

[1]Work for increasing $|\Delta\Gamma|$ by utilizing low-power active components can be found in [14], [15].

978-1-4799-4680-8/14/$31.00 ©2014 IEEE

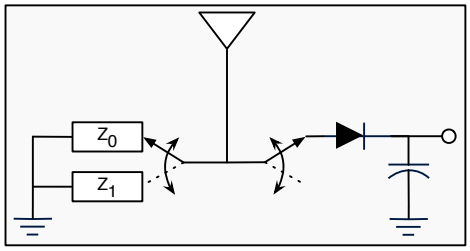

Fig. 1. Functionality of the 3-state RF front-end.

rectification circuit is required to convert the RF signals captured by the tag antenna to DC voltage that can drive the tag's digital logic and/or charging mechanism. The energy harvester input impedance has to be conjugate-matched to the antenna to guarantee maximum power transfer from the antenna to the rectifier.[2] This means that at state 0 (harvesting) the load at the antenna terminals is $Z_0 = Z_a^*$ and the reflection coefficient is $\Gamma_0 = 0$. If at state 1 (reflecting) the load is $Z_1 = \infty$ (open) and the reflection coefficient is $\Gamma_1 = 1$, then $|\Delta\Gamma| = 1$, which is suboptimal for backscatter communication. The same applies if $Z_1 = 0$ (short) and $\Gamma_1 = -1$.

The aforementioned show a tradeoff between the existence of a harvester on an RF tag (which could eliminate or minimize the requirements for an on-tag energy source) and optimized backscatter communication in terms of BER. The tradeoff is a result of the utilization of switching mechanisms that can only alternate between two load values (e.g. short/open or match/mismatch). Although a two-state switching mechanism such as a single transistor is a low-cost and low-power solution, the tradeoff of either employing a harvester or achieving optimized communication can be limiting in applications such as backscatter sensor networks that need to operate in long-ranges and at the same time employ the feature of "wirelessly charging" the sensor nodes' batteries.

In this work, a proof-of-concept RF front-end is described, which is capable of 3-state switching, at the cost of one additional transistor. The front-end's power consumption is still kept sufficiently low compared to its single-transistor counterpart, while the communication performance is boosted compared to a single-transistor match/mismatch modulator.

II. Front-end Design

A conventional RF tag front-end that utilizes a harvester would employ a switching mechanism to alternate the antenna load between the harvester and a reflective load (e.g. open). A 3-state front-end requires a switch for alternating between two load values for data modulation and a switch to turn the harvester on or off. A block diagram of this functionality is shown in Fig. 1. The main constraint for implementing a circuit with this functionality is keeping the dissipation power low, comparable to a single-switch circuit.

[2]An energy harvester is a non-linear network, whose input impedance is frequency- and power-dependent. This means that a perfect matching will occur at a specific frequency and power level. Typically, the power level where the matching occurs is small (under -10 dBm) [16].

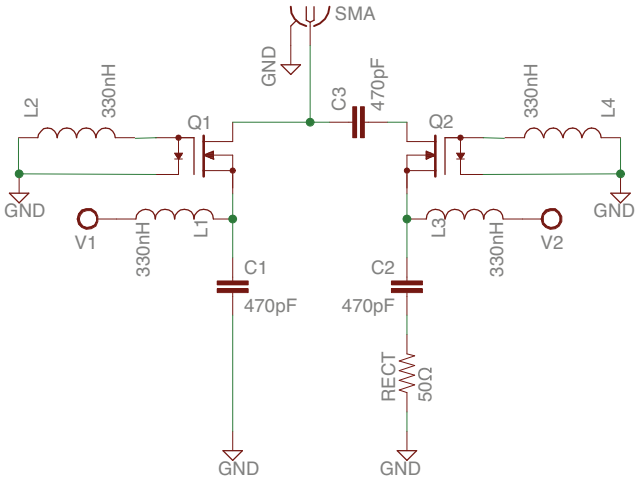

Fig. 2. Schematic of RF tag front-end.

A MOSFET transistor can be used to implement a low-cost, low-power switch. When properly biased, the transistor can ideally act as an open or a thru between the drain and source terminals. In that way, an antenna can be connected to the drain terminal and a load can be connected to the source terminal. When the transistor is 'on' the antenna load will be equal to the load connected to the source. When the transistor is 'off' the antenna load will be an 'open'. Moreover, if the source is connected directly to the ground instead of a load, when the transistor is 'on' the antenna load will be a 'short'. Thus, an open/short modulator can be built with just one MOSFET. In [8] the NXP BF1118 N-channel depletion-type MOSFET was used to implement a binary modulator. The same low-cost transistor with on-state insertion loss of ~ 2 dB and current consumption of 100 nA is used in this work.

The schematic of the front-end is shown in Fig. 2. Transistor Q1 is used as the modulator switch, while transistor Q2 is used as the harvester enable/disable switch. The transistors operate with a negative gate-source voltage (V_{GS}) and employ a diode in the same package, whose anode is internally connected to the transistor gate and the cathode is externally connected to the ground. The two transistors' inputs are the drain pins, and their outputs are the source pins. To achieve a negative V_{GS}, the gate of each transistor is grounded and a positive voltage is applied to the transistor source; for the modulator, the control voltage is V1, and for the harvester, the control voltage is V2. The control voltage low level is 0 V and the high level can be from 1.8 to 2.4 V. For preventing RF leakage into the DC sources, high-value inductors (330 nH) are placed between the control voltage input pins and the transistors' source pins, as well as between the gates and ground; the inductor impedance at the design frequency of 915 MHz is approximately $j1.9$ kΩ.

Biasing the transistor with a positive voltage on its source to achieve a negative V_{GS} yields a fundamental problem: an antenna short cannot be achieved by routing the antenna ground pin and the transistor source directly to the circuit board's 0 V ground plane, since this would mean that the 2 V bias would be directly connected to the 0 V ground. In other words, no common ground can be used for the DC and RF

signals. A workaround to this problem is using a separate RF ground plane which can have a floating DC potential of 2 V (or 0 V, according to the control voltage). However, although this solution is practical for a single-transistor open/short modulator, it is limiting for multi-transistor front-ends. An RF ground plane with a DC potential equal to a control voltage cannot be used, since there are multiple control voltages (one for each transistor) and each control voltage shall not be affected by other voltages. Another problem arises if the load connected to the transistor source is a harvester: the control voltage on the transistor source is going to be injected into the harvester's diode, producing unwanted results. Both of these problems can be solved by utilizing DC-block capacitors that will decouple the DC voltage from the ground or the load connected to the transistor's output. In Fig. 2, two DC-block capacitors (C1, C2) are placed at the transistors' outputs. The capacitance value has been selected to be high (470 pF) so that the impedance at 915 MHz is approximately $-j0.37\ \Omega$. For high-frequency signals, such a high-value capacitor can be seen as a short, and thus does not affect the RF path, while efficiently blocking the DC path. Another DC-blocking capacitor is placed between the two transistors' inputs to prevent DC leakage from one transistor's control voltage to the other transistor, which would produce unpredictable biasing.

The equivalent impedance of a rectifier matched to 50 Ω is shown in Fig. 2 as a resistor. For this work's testing circuit, an actual 50 Ω RF resistor has been utilized. For practical applications this resistor can be replaced with a harvester and its 50 Ω matching network.

III. Front-end Characterization

To accurately predict the performance of the fabricated circuit, Agilent ADS has been utilized for microwave analysis. To build the model of Fig. 2 in ADS, the S-parameters of the BF1118 transistor are needed, which are not readily available from the manufacturer. A device under test (DUT) consisting of the transistor and the two RF-reject inductors has been built for characterization (Fig. 3). The DUT is measured with a vector network analyzer (VNA) as a 2-port network (port 1: drain, port 2: source) and it is excited through microstrip feedlines. After calibration, the reference plane of the measurements is moved to the transistor's pins, to discard the microstrip line and SMA connector losses. From the VNA, the DUT S-parameters are obtained for 0 V, 1.8 V, and 2 V bias; the first corresponds to an 'on' transistor state, while the second and third correspond to the 'off' state. In practice, the S-parameters for any bias voltage over 1.8 V show negligible differences, which is a benefit when the supply voltage shows small fluctuations, or shows some small drop (e.g. in battery-operated systems). The extracted S-parameters are shown in Fig. 4. The 'off' state isolation (S_{21}) is approximately 17.8 dB and the 'on' state insertion loss (S_{21}) is approximately 1.8 dB across the 900–930 MHz UHF ISM band. The 'on' state return loss (S_{11}) is approximately -15.4 dB.

The characterization data are imported as S-parameter blocks in ADS for microwave simulation of the designed circuit. To accurately predict the front-end response, a full-wave simulation of the board layout has been conducted with

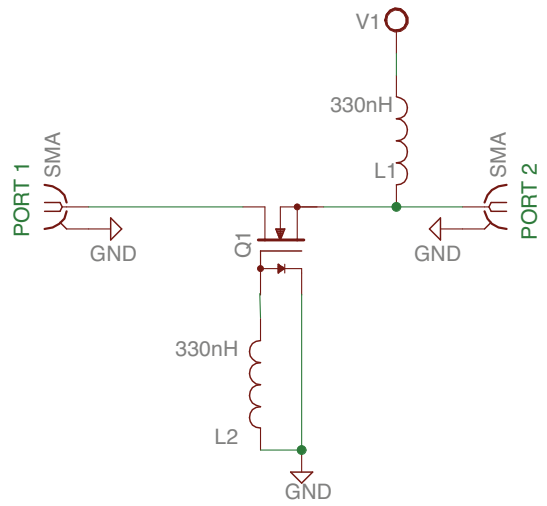

Fig. 3. Transistor characterization circuit.

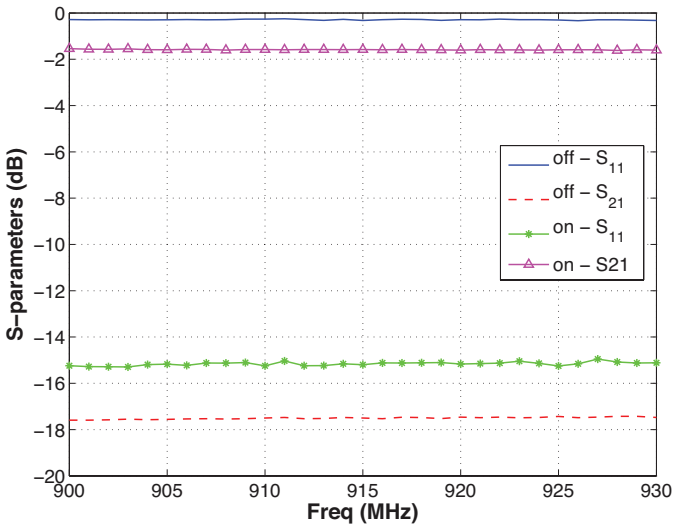

Fig. 4. Transistor measured S-parameters.

Momentum. In that way, all transmission line effects, as well as the surface mount device (SMD) interconnect parasitics are taken into account. The layout is designed using microstrip technology, with all components and transmission lines on the top board layer and a common ground plane at the bottom layer. Connections to the ground are implemented using vias. The layout is shown in Fig. 5, where the input microstrip line and the vias used for grounding the components can be seen. Notice that from the control input pads to the RF-reject inductors L1 and L3, thin lines are used, which have significantly higher characteristic impedance compared to the thick microstrip line present at the front-end input. The high mismatch to 50 Ω from the thin lines reinforces the RF-reject inductors and, thus, RF leakage towards the DC supplies is minimized. A co-simulation of the layout and circuit components is conducted to obtain the achievable $|\Delta\Gamma|$ values of the two-transistor front-end. For comparison, the $|\Delta\Gamma|$ values of a single-transistor front-end switching between the harvester and an open are also obtained by simulation.

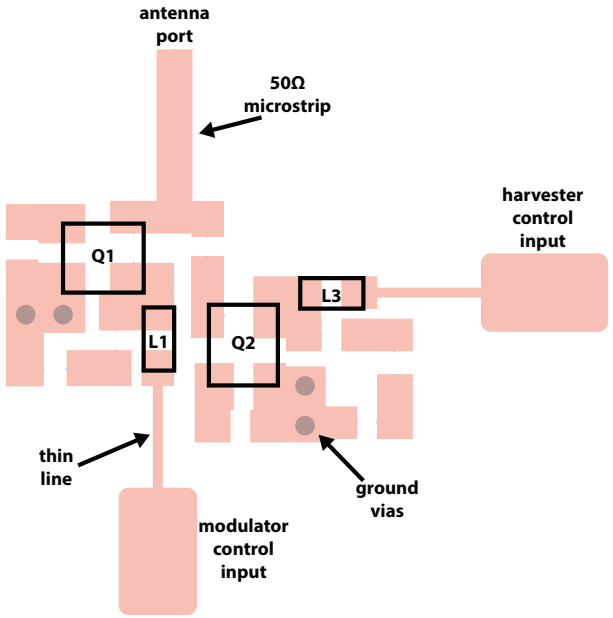

Fig. 5. Front-end board layout used in full-wave simulation.

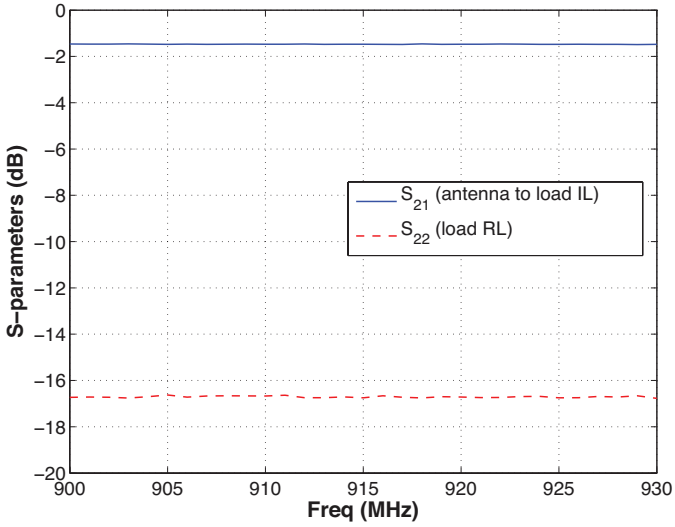

Fig. 6. Antenna to harvester transmission coefficient (IL) and mismatch at the harvester input (RL).

Since the aim along optimized communication is to achieve efficient RF harvesting, the performance of the harvesting part of the circuit is examined. The amount of power transferred from the antenna to the harvester input terminal is shown in Fig. 6. Here, port 1 refers to the antenna and port 2 refers to the 50 Ω load (matched harvester). Thus, S_{21} is the transmission coefficient, or insertion loss from the antenna to the harvester, which is ~ 1.8 dB. In the same figure, the mismatch, or return loss at the harvester input is shown. This mismatch is due to the use of a non-ideal transistor which a) shows a return loss on its terminals and b) acts as a lossy element between the 50 Ω antenna and the 50 Ω load. Without any matching, the return loss (S_{22}) at the transistor source (or the harvester input) is approximately -16.8 dB, which means that only 2% of the incident power at the harvester input is reflected back.

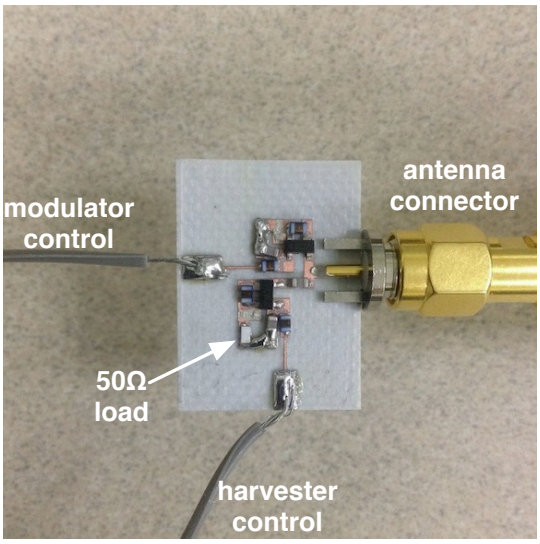

Fig. 7. RF front-end testing circuit.

TABLE I
RF FRONT-END STATES.

state	Q1(modulator)	Q2 (harvester)	ideal condition
S0	off	on	match
S1	on	off	short
S2	off	off	open

A front-end test circuit is fabricated on a double copper-clad Rogers RO4003C laminate with a dielectric constant $\epsilon_r = 3.55$, loss tangent $\tan\delta = 0.0021$, and substrate thickness 20 mil. The fabricated sample, which is shown in Fig. 7, is characterized with a VNA at the three different states shown in Table I. State 0 is the harvesting state and states 1, 2 correspond to modulator short and open, respectively. The three complex reflection coefficients are shown in Fig. 8. State 0 yields a reflection coefficient close to the center of the unitary circle, due to the 50 Ω load connected to transistor Q2 output. State 1 corresponds to a short circuit and would ideally produce a reflection coefficient of amplitude 1. However, due to the transistor 'on' state insertion loss, the reflection coefficient has a reduced amplitude, approximately 0.4. State 2 corresponds to an open, and thanks to the transistor's high 'off' state isolation, its amplitude is above 0.9. It is noted that the three reflection coefficients show small variation across the 900–930 MHz band, as it can be seen in Fig. 8.

To evaluate the enhanced communication performance of the designed front-end, two $|\Delta\Gamma|$ values are obtained by simulation and are verified by measurements. The first corresponds to a tag that switches between the harvester and an open state to modulate data (conventional tag):

$$|\Delta\Gamma_{\text{harvester}}| = |\Gamma(\text{harvester}) - \Gamma(\text{open})| \leq 1. \quad (4)$$

The second corresponds to a tag that switches between a short and an open to modulate data (proposed circuit):

$$|\Delta\Gamma_{\text{modulator}}| = |\Gamma(\text{short}) - \Gamma(\text{open})| \leq 2. \quad (5)$$

The two reflection coefficient distances are shown in Fig. 9,

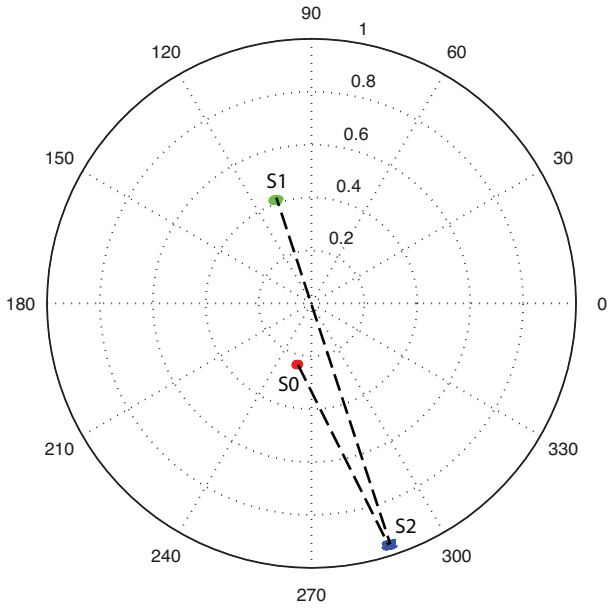

Fig. 8. Measured reflection coefficient values for the three different front-end states.

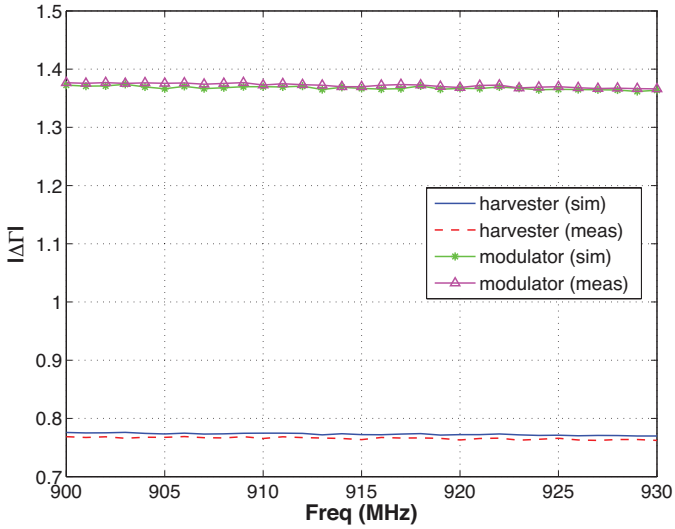

Fig. 9. Simulated and measured values for $|\Delta\Gamma|$.

both for simulations and measurements. Also, the distances can be represented as lines on the complex plane, which connect the two alternating reflection coefficients, as in Fig. 8. The distance achieved for the harvester/open front-end is 0.76, while the distance achieved for the short/open is 1.37. Thus the SNR values for the two front-ends are:

$$\mathrm{SNR}_{\mathrm{harvester}} \propto |\Delta\Gamma_{\mathrm{harvester}}|^2 = 0.58, \tag{6}$$

$$\mathrm{SNR}_{\mathrm{modulator}} \propto |\Delta\Gamma_{\mathrm{modulator}}|^2 = 1.88. \tag{7}$$

Then, the SNR gain for the second front-end is

$$\frac{\mathrm{SNR}_{\mathrm{modulator}}}{\mathrm{SNR}_{\mathrm{harvester}}} = 3.24 \rightarrow 5.1 \text{ dB}. \tag{8}$$

The aforementioned measurements give a comparison of two front-ends: a) one that employs a harvester and a single transistor for modulation, and b) one that employs a harvester, one transistor for modulation, and one transistor for harvester isolation. The second front-end clearly has a power dissipation that is double the power dissipation of the first front-end, since it utilizes two transistors instead of one. However, despite this excess power dissipation, the SNR gain at the reader is 5.1 dB, which can be valuable in long-range, low-SNR scenarios.

IV. Duty Cycle Requirements

It is common in sensor networks to employee a duty cycling scheme that consists of two states. During one state the sensor node is transmitting information, and during the other state the node remains idle. For example, a node that needs to convey a measurement to a central station every 1 hour will be at the communication state for a T_c seconds (the time depends on the communication bitrate and the data length) and at the idle state for $3600 - T_c$ seconds. For a harvester-equipped backscatter sensor node, the idle time also corresponds to harvesting time, i.e. while the node does not transmit any information, it is collecting and storing energy that is needed for the actual transmission.

To investigate the duty cycle requirements of the front-end of this work, a comparison can be made with a conventional harvester-equipped front-end. The latter consists of a harvesting cycle and a communication cycle; during the communication cycle, it switches between the harvester and a reflective load. This means that on average, half of the communication time also corresponds to harvesting time. So the actual harvesting extends beyond the harvesting-only cycle. The front-end of this work consists of a harvesting-only cycle and a communication-only cycle. Harvesting during communicating is not possible for this front-end since the switching occurs between two reflective loads.

Assume that the conventional tag communication bitrate is R_b and the bit duration is $T_b = 1/R_b$. For a data packet of N_b bits, the total communication time is $T_c = N_b\ T_b$. The energy required for communication is

$$E_c = P_c\ T_c, \tag{9}$$

where P_c is the power dissipation of the conventional single-switch front-end. Assuming that a harvester is capable of providing power P_h, the total harvested energy is

$$E_h = P_h \left(T_h + \frac{1}{2} T_c \right), \tag{10}$$

where T_h is the harvesting-only cycle time. The factor $T_c/2$ accounts for the fact that harvesting also occurs during half of the communication time. Assuming that all of the harvested energy is utilized for communication, the expression

$$E_h = E_c \tag{11}$$

yields the required harvesting time for a given communication time T_c

$$T_h = \left(\frac{P_c}{P_h} - \frac{1}{2} \right) T_c. \tag{12}$$

The total time required for one packet transmission is

$$T_{\text{total}} = T_h + T_c = \left(\frac{P_c}{P_h} + \frac{1}{2}\right) T_c. \quad (13)$$

This work's front-end design dissipates double the power (since it employs two switches) and is able of collecting energy only during the harvesting cycle. Thus,

$$E'_c = 2P_c\ T'_c, \quad (14)$$

$$E'_h = P_h\ T'_h. \quad (15)$$

Then, the harvesting time required is

$$T'_h = \frac{2P_c}{P_h}\ T'_c, \quad (16)$$

and the total time for one packet is

$$T'_{\text{total}} = T'_h + T'_c = \frac{2P_c}{P_h}\ T'_c. \quad (17)$$

For a fixed packet rate between the two front-ends,

$$T_{\text{total}} = T'_{\text{total}} \Rightarrow T'_c = \frac{T_c}{2}, \quad (18)$$

i.e. the communication time has to be halved. This essentially means that the communication bitrate has to be doubled to convey the same data packet of N_b bits to the reader. From Eq. (3) it can be seen that a bitrate doubling will cause a 3 dB SNR drop. The SNR gain of the designed front-end is 5.1 dB, as described in the end of Sec. III, and thus the total SNR gain at the reader for a fixed packet rate will be $5.1\text{ dB} - 3\text{ dB} = 2.1\text{ dB}$.

If there is a fixed bitrate (and not packet rate) requirement, the SNR gain will be 5.1 dB, according to Eq. (3) and Sec. III front-end performance analysis. The required harvesting time for this work's front-end compared to the harvesting time of the conventional tag will then be

$$T'_h = \frac{2P_c}{P_h}\ T_c = \frac{4P_c}{2P_c - P_h}\ T_h. \quad (19)$$

Notice that in the above simplified analysis, only the power dissipation of the front-end circuit has been taken into account. This neglects the power dissipation of the control circuitry (in the form of a microcontroller) and sensors. In practice, the power dissipation of the control logic (on the order of mW) will overwhelm the power dissipation of the front-end (on the order of nW) and thus, the required harvesting time for a tag equipped with this work's front-end will not be significantly higher than that of a tag equipped with a conventional front-end. As a result, the bitrate difference between the two different tag front-ends will be small for a fixed duty cycle and the SNR loss due to bitrate increase will be significantly lower than 3 dB. This means that the SNR gain of a front-end with two switches will approach 5.1 dB for practical scenarios.

V. Conclusion

In this work, a proof-of-concept RF front-end has been designed, analyzed, and implemented for employing energy harvesting mechanisms on backscatter radio communicators without compromising their communication performance. Having the constraints for optimized backscatter communication in mind, a low-power circuit has been proposed, that efficiently expands the functionality of previously-developed RF tag front-ends based on transistor switches. Simulation and measurement results have been provided for the front-end performance, and the SNR gain of the proposed front-end has been evaluated. Improvements on the performance of this system could be possible through the utilization of lower loss RF switches based on CMOS technology. Nevertheless, although the transistors utilized in this work show non-negligible losses, their ultra low-power operation and low monetary cost make them appealing for backscatter sensors in large-scale wireless sensor network applications.

References

[1] *EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID Protocol for Communications at 860MHZ–960MHZ, version 1.2.0*. EPC Global, 2008.

[2] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards, Radio Frequency Identification and Near-Field Communication*, 3rd ed. New York, NY, 10158: John Wiley & Sons, Inc., 2010.

[3] V. Lakafosis, A. Traille, H. Lee, E. Gebara, M. M. Tentzeris, G. R. DeJean, and D. Kirovski, "RF fingerprinting physical objects for anticounterfeiting applications," *IEEE Trans. Microwave Theory Tech.*, vol. 59, no. 2, pp. 504–514, 2011.

[4] G. Vannucci, A. Bletsas, and D. Leigh, "A software-defined radio system for backscatter sensor networks," *IEEE Trans. Wireless Commun.*, vol. 7, no. 6, pp. 2170–2179, Jun. 2008.

[5] A. Sample, D. Yeager, P. Powledge, and J. Smith, "Design of a passively-powered, programmable sensing platform for UHF RFID systems," in *Proc. IEEE RFID Conf.*, Grapevine, TX, Mar. 2007, pp. 149–156.

[6] V. Lakafosis, A. Rida, R. Vyas, L. Yang, S. Nikolaou, and M. M. Tentzeris, "Progress towards the first wireless sensor networks consisting of inkjet-printed, paper-based RFID-enabled sensor tags," *Proc. IEEE*, vol. 98, no. 9, pp. 1601–1609, Sep. 2010.

[7] J. Kimionis, A. Bletsas, and J. N. Sahalos, "Design and implementation of RFID systems with software defined radio," in *6th IEEE European Conf. on Antennas and Propagation (EuCAP)*, Prague, Czech Republic, Mar. 2012, pp. 3464–3468.

[8] E. Kampianakis, J. Kimionis, K. Tountas, C. Konstantopoulos, E. Koutroulis, and A. Bletsas, "Backscatter sensor network for extended ranges and low cost with frequency modulators: Application on wireless humidity sensing," in *Proc. IEEE Sensors 2013*, Baltimore, MD, Nov. 2013.

[9] D. M. Dobkin, *The RF in RFID: Passive UHF RFID in Practice*. Newnes (Elsevier), 2008.

[10] J. D. Griffin and G. D. Durgin, "Complete link budgets for backscatter-radio and RFID systems," *IEEE Antennas Propagat. Mag.*, vol. 51, no. 2, pp. 11–25, Apr. 2009.

[11] A. Bletsas, A. G. Dimitriou, and J. N. Sahalos, "Improving backscatter radio tag efficiency," *IEEE Trans. Microwave Theory Tech.*, vol. 58, no. 6, pp. 1502–1509, Jun. 2010.

[12] J. Kimionis, A. Bletsas, and J. N. Sahalos, "Bistatic backscatter radio for tag read-range extension," in *IEEE Int. Conf on RFID-Technologies and Applications (RFID-TA)*, Nice, France, Nov. 2012, pp. 356–361.

[13] J. Kimionis, A. Bletsas, and J. N. Sahalos, "Increased range bistatic scatter radio," *IEEE Trans. Commun.*, vol. 62, no. 3, pp. 1091–1104, Mar. 2014.

[14] J. Kimionis, A. Georgiadis, S. Kim, A. Collado, K. Niotaki, and M. M. Tentzeris, "An enhanced-range RFID tag using an ambient energy powered reflection amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig. (IMS)*, Tampa Bay, FL, Jun. 2014.

[15] J. Kimionis, A. Georgiadis, A. Collado, and M. M. Tentzeris, "Inkjet-printed reflection amplifier for increased-range backscatter radio," in *European Microwave Conference (EuMC)*, Rome, Italy, Oct. 2014.

[16] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7μW minimum RF input power," *IEEE J. Solid-State Circuits*, pp. 1602–1608, Oct. 2003.