A Novel Compact Isolation Circuit Suitable for Ultracompact and Wideband Marchand Baluns

Hee-Ran Ahn, *Senior Member, IEEE*, and Manos M. Tentzeris, *Fellow, IEEE*

***Abstract*—A novel compact isolation circuit (IC) is proposed for the ultracompact and wideband UHF Marchand balun topology, and exact design formulas are presented for arbitrary coupling coefficients and impedance-transforming termination impedances. The wideband Marchand balun mainly consists of two identical coupled transmission-line sections which are far shorter than 90° long, connecting segment, two or three lumped elements and the proposed IC. The novel IC features −180° phase delay between two balanced ports, and makes the ultracompact implementation possible, which is quite different from the conventional ones with 180° phase delays between two balanced ports. In addition, due to the −180° phase delays, excellent isolation performance and excellent phase responses can be performed. For the proof-of-concept demonstrations, one prototype with each coupled-line section being only 20° long and the half IC being only 20° long is tested at 700 MHz. The measured frequency responses are in good agreement with the predicted ones with the performance of the 10-dB return loss bandwidth of 40% and −15 dB isolation bandwidth of 121.4%. In terms of sizes versus bandwidths, the fabricated Marchand balun can be regarded as the best and the smallest ever recorded, based on the low-cost microstrip technology.**

***Index Terms*—Marchand baluns, compact Marchand baluns, connecting segments for Marchand baluns, near-perfect isolation, power dividers, ultracompact wideband Marchand baluns.**

I. Introduction

THE MARCHAND balun [1], consisting of two identical 90° coupled transmission-line sections (CPLs), transforms unbalanced signals into balanced ones [2], [3] and functions as a power divider which requires near-perfect isolation and matching at two balanced ports. As numerous multifunctional wireless modules require a substantial reduction in mass and volume, the compactness of the Marchand baluns has been of high interest, and various compact (miniaturized) Marchand baluns have been reported [4]–[12]. However, due to the lack of design rules for the connecting segment between the two CPLs, the Marchand baluns [4], [5] can be implemented only in multilayer configurations. Other Marchand balun topologies with CPLs that are much shorter than 90° do not give the design formulas [6]. Only optimization method using tuning bars [7] is possible, and only approximate analysis [8] for the connecting segment is possible, and the bandwidths [9], [12] are very small. Furthermore, even with the disadvantages mentioned above, all the works [4]–[12] cannot be designed with near-perfect isolation and near-perfect matching at the balance ports, because it is very difficult to design the isolation circuits (ICs) for the compact topologies [2]. The isolation circuits for the Marchand baluns are available in [3], [13], [14], but the sizes are not compact along with unfeasibility for the conventional compact baluns.

To overcome these problems, a novel ultracompact wideband Marchand balun is suggested. For this, a novel compact IC is proposed, featuring −180° phase difference between two balanced outputs, which is quite different from the conventional ones having 180° phase difference between those ports.

In detail, this brief introduces a novel topology of a ultracompact Marchand balun consisting of two CPLs that can be far shorter than 90° long, a connecting segment and the proposed novel IC introducing negative electrical lengths with accurate design formulas. Due to −180° phase delays between two balanced ports, excellent isolation performance and excellent phase responses can be achieved. To verify the suggested theory, one prototype with CPLs that are only 20° long at 700 MHz was tested. The measured results are in good agreement with the prediction with the performance of the 10-dB return loss bandwidth of 40% and −15-dB isolation bandwidth of 121.4%. In terms of sizes versus bandwidths, the fabricated prototype can be regarded as the best and the smallest ever recorded, based on the low-cost microstrip technology.

II. Ultracompact Marchand Baluns

The typical Marchand balun topology with the termination impedances of Z_r at port ① and Z_L at ports ② and ③ is depicted in Fig. 1(a) where it consists of two identical 90° CPLs and an IC. The design formulas for the even- and odd-mode admittances Y_{eR} and Y_{oR} of the 90° CPLs in Fig. 1(a) [3] are

$$Y_{eR}{}^{-1} = Z_{eR} = \sqrt{2Z_rZ_L}\,\frac{C_0}{1-C_0} \tag{1a}$$

$$Y_{oR}{}^{-1} = Z_{oR} = \sqrt{2Z_rZ_L}\,\frac{C_0}{1+C_0} \tag{1b}$$

where C_0 is the coupling coefficient of the 90° CPLs. Since the two CPLs are connected together in Fig. 1(a), to make ports ② and ③ and build an IC are extremely difficult. So, the connecting segment between two CPLs is necessary. For this purpose, replacing each 90° CPL with the mixed equivalent circuit in

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The authors are with the school of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: hranahn@gmail.com; etentze@ece.gatech.edu).

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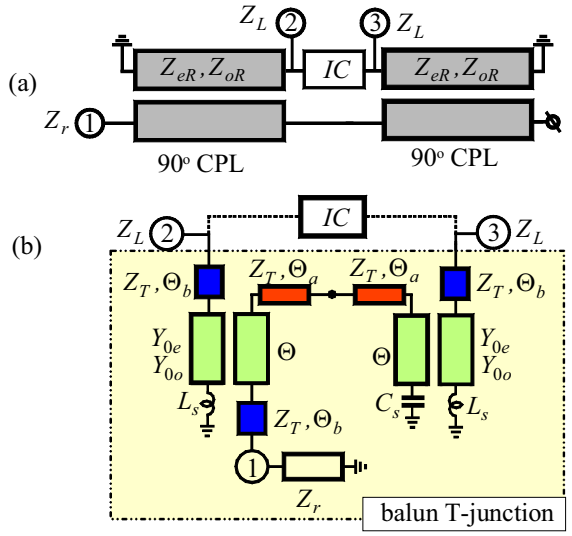

Fig. 1. Marchand balun and its ultracompact Marchand balun (UM). (a) Marchand balun. (b) UM.

[14, Fig. 2(c)] gives the ultracompact marchand balun (UM) configuration depicted in Fig. 1(b).

The UM consists of two sets of CPLs with the even- and odd-mode admittances of Y_{0e} and Y_{0o} and the electrical length of Θ, a connecting segment with the characteristic impedance of Z_T and the electrical length of $2\Theta_a$, three identical transmission-line sections (TLs) with the characteristic impedance Z_T and the electrical length Θ_b and inductors of L_s and a capacitor of C_s where

$$\omega L_s = Z_T \tan\Theta_a \tag{2a}$$

$$\omega C_s = Y_T \tan\Theta_b \tag{2b}$$

$$Z_T = {Y_T}^{-1} = \sqrt{Z_{eR}Z_{oR}} \tag{2c}$$

The design formulas for Y_{0e}, Y_{0o}, Θ of the mixed equivalent circuit in [14] are given as

$$Y_{0e} = Y_T\sqrt{\frac{{G_e}^2 - {Y_T}^2\ tan^2\Theta_b - 2G_eY_T\ \tan\Theta_b\cot\Theta_g}{{Y_T}^2 - {G_e}^2tan^2\Theta_b - 2G_eY_Ttan\Theta_b\cot\Theta_g}} \tag{3a}$$

$$Y_{0o} = Y_T\sqrt{\frac{{G_o}^2 - {Y_T}^2\ tan^2\Theta_b - 2G_oY_T\ \tan\Theta_b\cot\Theta_g}{{Y_T}^2 - {G_o}^2tan^2\Theta_b - 2G_oY_Ttan\Theta_b\cot\Theta_g}} \tag{3b}$$

$$\tan\frac{\Theta}{2} = \sqrt{\frac{\left(Y_T - G_e\ cot\frac{\Theta_g}{2}\tan\Theta_b\right)\left(G_e\ tan\frac{\Theta_g}{2} - Y_T\ \tan\Theta_b\right)}{\left(Y_T + G_e\ tan\frac{\Theta_g}{2}\tan\Theta_b\right)\left(G_e\ cot\frac{\Theta_g}{2} + Y_T\ \tan\Theta_b\right)}} \tag{3c}$$

where

$$\cos\Theta_g = j\frac{\left({Y_T}^2 - {A_m}^2\right)}{Y_Tcsc\Theta_dA_p} \tag{3d}$$

$$G_e = \frac{-j\left({Y_T}^2csc\Theta_d\right)\left(A_pcot\Theta_d + A_mcsc\Theta_d\right)\sin\Theta_g}{{Y_T}^2\cot^2\Theta_d + {A_m}^2} \tag{3e}$$

$$G_o = \frac{-j\left({Y_T}^2csc\Theta_d\right)\left(A_pcot\Theta_d - A_mcsc\Theta_d\right)\sin\Theta_g}{{Y_T}^2\cot^2\Theta_d + {A_m}^2} \tag{3f}$$

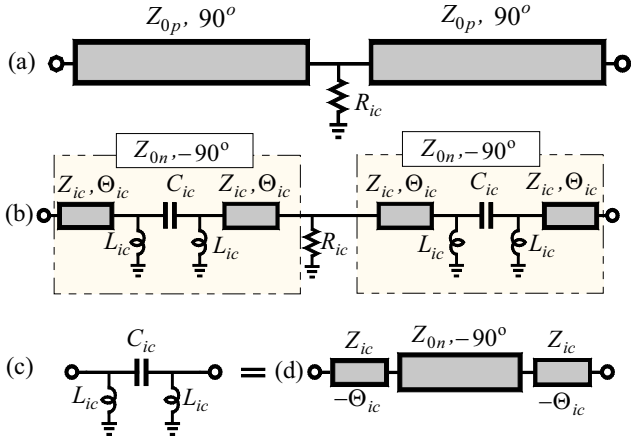

Fig. 2. ICs. (a) Conventional IC. (b) Novel IC. (c) Equivalent circuit of Π−type lumped elements.

$$A_p = j\frac{(Y_{eR} + Y_{oR})}{2}\ ,\ A_m = j\frac{(Y_{eR} - Y_{oR})}{2} \tag{3g}$$

where $\Theta_d = \Theta_a - \Theta_b\ > 0°$ with $\Theta_a > 0°$ and $\Theta_b \geq 0°$. If $\Theta_b = 0°$ is designed, the sizes can be reduced further.

III. Novel Compact Isolation Circuits

The IC of the UM in Fig. 1(b) is the same as that of the conventional one in Fig. 1(a), because the design formulas in (3) were derived from the condition that both circuit parameters in Fig. 1(a) and (b) are the same at the design frequency. The admittance parameters of the balun T-junction in Fig. 1(b) [15] are

$$\begin{bmatrix} i_2 \\ i_3 \end{bmatrix} = \frac{1}{2Z_L}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_2 \\ v_3 \end{bmatrix} \tag{4}$$

where i_2 and i_3 are the currents at ports ② and ③, while v_2 and v_3 are the voltages at both ports. For the perfect matching at both ports and the perfect isolation between the balance ports, those of the IC [15], [16] should be

$$\begin{bmatrix} i_2 \\ i_3 \end{bmatrix} = \frac{1}{2Z_L}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} v_2 \\ v_3 \end{bmatrix} \tag{5}$$

The admittance parameters (5) indicate that the phase delay between ports ② and ③ in Fig. 1 should be ±180°, leading to several possible topologies. One of them for +180° phase delay between the ports is that in Fig. 2(a), consisting of two identical 90° TLs with the arbitrary values of characteristic impedances of Z_{0p} and an isolation resistance of R_{ic}. However, the conventional IC in Fig. 2(a) can't be implemented with the UM, because of the restriction on the compactness. To improve the shortcomings, the novel IC is suggested in Fig. 2(b), consisting of two identical TLs with the characteristic impedance of Z_{0n} but the electrical length of −90° and the isolation resistor of R_{ic}. The relation between Z_{0n}, R_{ic} and Z_L is

$$Z_{0n} = {Y_{0n}}^{-1} = \sqrt{2Z_LR_{ic}} \tag{6}$$

Each −90° TL can be reduced to one Π−type lumped elements with C_{ic} and L_{ic} and two identical TLs with the characteristic impedance of Z_{ic} and the electrical length of

TABLE I
DESIGN PARAMETERS FOR $Z_r = Z_L = 50\ \Omega$

R_{ic}= 30 Ω, $\Theta_{ic} = 5^o$, $Z_{ic} = 54.77\ \Omega$, $C_{ic} = 4.2$ pF , $L_{ic} =$ 10.5 nH in Fig. 2(b)	
C_0 = -6 dB ($Z_{eR} = 71\ \Omega$, $Z_{oR} = 23.6\ \Omega$, $Z_T = 41\ \Omega$)	
$\Theta_a = 50^o$, $\Theta_b = 0^o$	$Z_{0e} = 116\ \Omega$, $Z_{0o} = 14.4\ \Omega$, $\Theta = 27.7^o$, $L_s = 11$ nH, $C_s = 0$ pF
$\Theta_a = 42^o$, $\Theta_b = 9^o$	$Z_{0e} = 121.6\ \Omega$, $Z_{0o} = 13.8\ \Omega$, $\Theta = 26.1^o$, $L_s = 8.38$ nH, $C_s = 0.88$ pF

Θ_{ic} as shown in Fig. 2(b). The two TLs are as short as possible and only for soldering purpose of the lumped elements. The design formulas can be derived by connecting two identical TLs with Z_{ic} and $-\Theta_{ic}$ to both sides of each $-90°$ TL, leading to the relation in Fig. 2(c) and (d). The even- and odd-mode admittances of both circuits in Fig. 2(c) and (d) are

$$Y_{ev\_L} = \frac{1}{j\omega L_{ic}}, \quad Y_{od\_L} = \frac{1}{j\omega L_{ic}} + j2\omega C_{ic} \tag{7a}$$

$$Y_{ev\_S} = -jY_{ic}\frac{Y_{0n} + Y_{ic}\tan\Theta_{ic}}{Y_{ic} - Y_{0n}\tan\Theta_{ic}} \tag{7b}$$

$$Y_{od\_S} = -jY_{ic}\frac{-Y_{0n} + Y_{ic}\tan\Theta_{ic}}{Y_{ic} + Y_{0n}\tan\Theta_{ic}} \tag{7c}$$

where $Y_{ic} = {Z_{ic}}^{-1}$, Y_{ev_L} and Y_{od_L} are the even- and odd-mode input admittances in Fig. 2(c), while Y_{ev_S} and Y_{od_S} are those of the stepped impedance TLs in Fig. 2(d). By equating $Y_{ev\_L} = Y_{ev\_S}$ and $Y_{od\_L} = Y_{od\_S}$, the design formulas for ωL_{ic} and ωC_{ic} can be derived as

$$\omega L_{ic} = \frac{Y_{ic} - Y_{0n}\tan\Theta_{ic}}{Y_{ic}(Y_{ic}\tan\Theta_{ic} + Y_{0n})} \tag{8a}$$

$$\omega C_{ic} = \frac{Y_{0n}{Y_{ic}}^2\sec^2\Theta_{ic}}{{Y_{ic}}^2 - {Y_{0n}}^2\tan^2\Theta_{ic}}. \tag{8b}$$

IV. DESIGNS AND FREQUENCY RESPONSES

For the designs of the UMs, the first thing is to design IC, and the isolation resistor R_{ic} can be determined arbitrarily, depending on available chip resistance values. If the value of R_{ic} is selected as 30 Ω, $Z_{0n} = 54.77\ \Omega$ is calculated from (6) with fixing at $Z_L = 50\ \Omega$. If $Z_{ic} = 54.77\ \Omega$ and $\Theta_{ic} = 5°$ in Fig. 2(b) are selected arbitrarily, the rest values of C_{ic} and L_{ic} can be calculated as $C_{ic} = 4.2$ pF, $L_{ic} = 10.5$ nH at 0.7 GHz. The next is to design the rest circuit of the UM using the design formulas in (1)-(3). For this, the coupling coefficient of C_0 can be determined arbitrarily as $C_0 = -6$ dB, leading to $Z_{eR} = 71\ \Omega$, $Z_{oR} = 23.6\ \Omega$, and $Z_T = 41\ \Omega$. Then, for the electrical lengths of Θ less than 30°, two cases for $(\Theta_a, \Theta_b) = (50°, 0°)$ and (42°, 9°) can be determined by sweeping $\Theta_d = \Theta_a - \Theta_b$. The design parameters for two UMs are collected in Table I where the first row parameters are for the novel IC in Fig. 2(b).

To highlight the advantage of the novel IC in Fig. 2(b), frequency responses with the conventional IC in Fig. 2(a), and novel ICs are compared for $\Theta_a = 42°$ and $\Theta_a = 50°$ in Fig. 3 where the conventional IC is only for $\Theta_a = 50°$. In this case, the total length of the novel IC is only 20°, while that

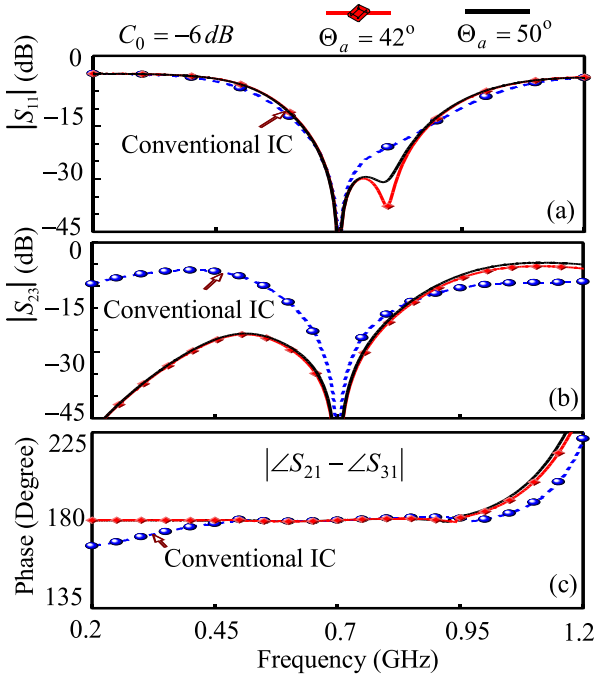

Fig. 3. Compared frequency responses for C_0= −6 dB. (a) $|S_{11}|$. (b) $|S_{23}|$. (c) Phase difference of $|\angle S_{21} - \angle S_{31}|$.

of the conventional IC is 180° with $Z_{0p} = Z_{0n}$. The scattering parameters of $|S_{11}|$ and $|S_{23}|$ are plotted in Fig. 3(a) and (b), respectively, while the phase differences of $|\angle S_{21} - \angle S_{31}|$ are in Fig. 3(c) where the design frequency is 700 MHz. The frequency responses for $\Theta_a = 42°$ and $\Theta_a = 50°$ are expressed with red and black solid lines, respectively, and the dotted blue responses are those with the conventional IC. The electrical lengths of Θ are 27.7° and 26.1° for $\Theta_a = 50°$ and $\Theta_a = 42°$, respectively as can be seen in Table I. The two frequency responses with the novel IC are about the same, because of about the same electrical lengths of Θ and the same value of $C_0 = -6$ dB. However, the responses with the novel IC are much better than those with the conventional IC, especially in the isolation performance and the phase responses in Fig. 3(b) and (c), respectively.

V. VERIFICATION AND COMPARISONS

For the verification of the suggested theory, one prototype was designed at 700 MHz and fabricated on the substrate (RT/duroid 5870, $\epsilon_r = 2.33$, $H = 31$ mil, $\tan\delta = 0.0012$).

A. Fabrication and Frequency Responses

For the prototype, $\Theta_a = 54.4°$ and $\Theta_b = 0°$ were selected for $C_0 = -6$ dB and $\Theta = 20°$, leading to the calculation values of $Z_{0e} = 149.8\ \Omega$, $Z_{0o} = 11.19\ \Omega$, $L_s = 13$ nH, and $C_s = 0$ pF. In this case, $Z_T = 41\ \Omega$. Due to too low value of Z_{0o} to fabricate with 2D CPL, too high value of coupling coefficient, 3D CPL with VIP (vertically installed planar) [14], [17], [18] is demanded as depicted in Fig. 4(a) where the dielectric constants of the substrate and the VIP are indicated differently as ϵ_r and ϵ_{rv}, the height of the VIP is specified as w_v, the widths of the two identical conductor lines are w_c, and

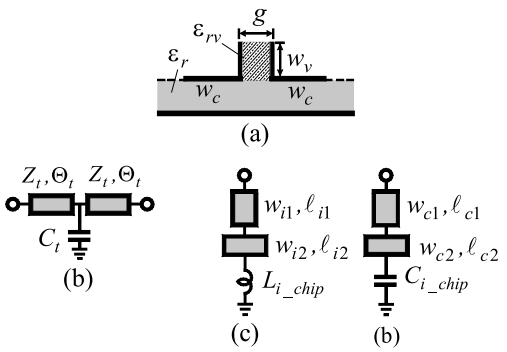

Fig. 4. (a) 3D CPL. (b) T-type (c) Fabrication of required inductance. (c) Fabrication of required capacitance.

the gap is g. The connecting segment of a TL with Z_T and $2\Theta_a$ in Fig. 1(b) should be reduced to T-types with N [3], and a T-type is depicted in Fig. 4(b), consisting of two identical TLs with the characteristic impedance of Z_t and Θ_t and one shunt capacitance of C_t. Since the inductance and capacitance values of the chip inductors and capacitors are limited, the required inductance and capacitance values cannot be fabricated with available chip inductor or capacitor only, and soldering is also a problem. So the inductance should be implemented with two TLs and an available chip inductor (L_{i_chip}) as shown in Fig. 4(c) where the widths and lengths of the first and second TLs are (w_{i1} and ℓ_{i1}) and (w_{i2} and ℓ_{i2}), respectively. For the required capacitance implementation, two TLs (w_{c1} and ℓ_{c1}) and (w_{c2} and ℓ_{c2}) and an available chip capacitor (C_{i_chip}) can be applied as well in Fig. 4(d). The subscript of i for L_{i_chip} and C_{i_chip} is meant as s, t and ic for L_s in Fig. 1(b), C_t for the T-type in Fig. 4(b) and L_{ic} of the IC Fig. 2(b).

For the 3D CPLs, first consider $Z_{0e} = 149.8\ \Omega$ and $Z_{0o}{}' = 91.5\ \Omega$ where Z'_{0o} is the odd-mode impedance for 2D CPL in [14, eq. (23)] to fix width w_c and gap g at $w_c = 0.4$ mm and $g = 0.5$ mm. Since the required odd-mode impedance is 11.19 Ω, the odd-mode impedance produced by the VIP [14, Fig. 18(b)] should be 12.75 Ω so that the parallel connection of 91.5 Ω and 12.75 Ω can be 11.19 Ω. In a similar way to [14], the length of w_v of the VIP in Fig. 4(a) can be estimated as $w_v = 3.49$ mm for $\epsilon_{rv} = 3.38$. To make use of available chip capacitors with $C_{ic} = 3.9$ pF for the IC, $R_{ic} = 40\ \Omega$, $Z_{ic} = 80\ \Omega$ and $\Theta_{ic} = 10°$ were selected. Then L_{ic} was calculated as $L_{ic} = 9.8$ nH at 0.7 GHz.

The design and fabrication parameters are collected in Table II. To realize $L_s = 13$ nH, a chip inductor with 12 nH was soldered with two TLs, and the characteristic impedance and the electrical length of the first TL in Fig. 4(c) are 140 Ω and 0.7°, while those of the second one are 70 Ω and 1.28°. For $C_t = 3$ pF of the T-type in Fig. 4(b), the available chip capacitor with $C_{t\_chip} = 2.7$ pF was soldered, and those of the two TLs in Fig. 4(d) are (120 Ω, 1°) and (50 Ω, 1.75°). For $L_{ic} = 9.8$ nH, available chip inductors with 8.2 nH were soldered with two TLs having (130 Ω, 2°) and (60 Ω, 1.17°). The fabricated prototype and detailed layouts are illustrated in Fig. 5 where the whole layout, the connecting segment and IC are detailed in Fig. 5(a), (b) and (c), respectively, while the

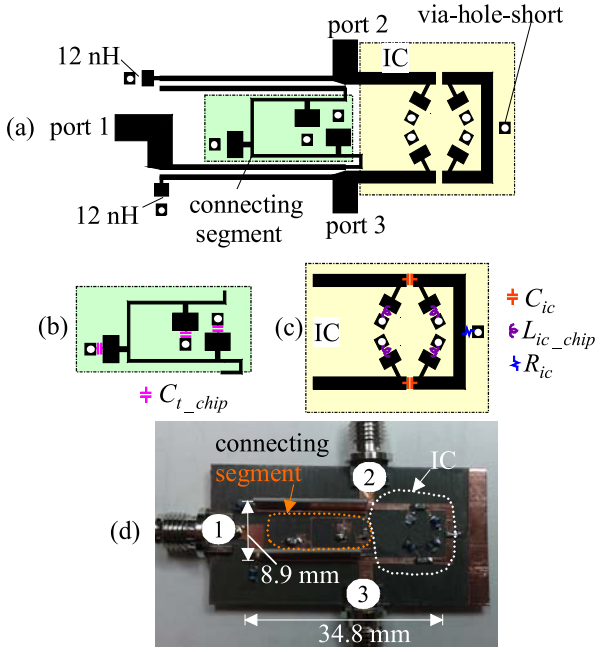

Fig. 5. Fabricated prototype. (a) Whole Layout. (b) Detailed connecting segment. (c) Detailed IC. (d) Fabricated prototype.

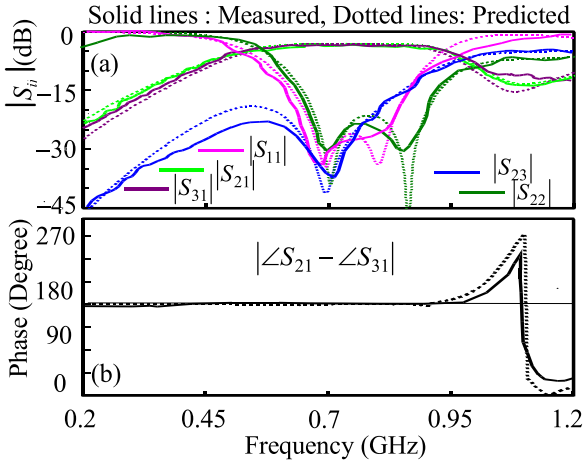

Fig. 6. Compared simulated and measured frequency responses. (a) $|S_{11}|$, $|S_{21}|$, $|S_{31}|$, $|S_{22}|$ and $|S_{23}|$. (b) Phase responses of $|\angle S_{21} - \angle S_{31}|$.

fabricated prototype is in Fig. 5(d) where the CPLs are each only 20° long.

The measured and predicted frequency responses are compared in Fig. 6(a) and (b) where the measured $|S_{11}|$, $|S_{21}|$ and $|S_{31}|$ at 0.7 GHz are −34.2 dB, −3.28 dB and −3.32 dB, respectively, while $|S_{22}|$ and $|S_{23}|$ are −30.02 dB and −35.8 dB, respectively, and the phase difference between S_{21} and S_{31} is 181.27°. Very good agreement between the measured and the simulated/predicted responses can be easily observed.

B. Comparisons With Conventional Works

The calculated values for the occupied size without the isolation circuits are compared with various other state-of-the-art conventional implementations in Table III, because no isolation circuit exists in [7], [9], [10], [12].

TABLE II
DESIGN AND FABRICATION PARAMETERS FOR PROTOTYPE

$Z_{0e} = 149.8\,\Omega$, $Z_{0o} = 11.19\,\Omega$, $\Theta = 20^{o}$, $L_s = 13$ nH, $C_s = 0$ pF.
$w_c = 0.4$ mm, $g = 0.5$ mm, $\ell_c = 17.8$ mm, w_v =3.49 mm (ε_{rv}=3.38) $L_{s\_chip} = 12$ nH, $w_{i1} = 0.27$ mm, $\ell_{i1} = 0.62$ mm, $w_{i2} = 1.35$ mm, $\ell_{i2} = 1.1$ mm
Connecting segment ($Z_T = 40.95\,\Omega$, $2\Theta_a = 108.8^{o}$) → 3 *T-type = 3*($Z_t = 147.36\,\Omega$, $\Theta_t = 5.2^{o}$, C_t =3 pF)
$w_t = 0.23$ mm, ℓ_t =4.65 mm, $C_{t\_chip} = 2.7$ pF, $w_{c1} = 0.42$ mm, $\ell_{c1} = 0.9$ mm, $w_{c2} = 2.33$ mm, $\ell_{c2} = 1.48$ mm
IC : $R_{ic} = 40\ \Omega$, Z_{ic} =80 Ω, $\Theta_{ic} = 10^{o}$, $C_{ic} = 3.9$ pF, L_{ic} = 9.8 nH.
$w_{ic} = 1.1$ mm, $\ell_{ic} = 8.67$ mm, $L_{ic\_chip} = 8.2$ nH, w_{i1} = 0.27 mm, $\ell_{i1} = 1.78$ mm, $w_{i2} = 1.75$ mm, $\ell_{i2} = 1.0$ mm

TABLE III
COMPARISONS WITH VARIOUS MARCHAND BALUNS

	This work	[7]	[9]	[10]	[12]
Size	200	6627	1062	1600	1240
Isolation %	121.4	No	No	No	No
S_{11} %	40	24	30	40	18.75
Amp (dB)	0.65	0.5	0.39	0.5	0.19
Phase imb.	1.2^{o}	1^{o}	10^{o}	1.5^{o}	0.82^{o}
f_0 (GHz)	0.7	59	2.45	1.4	2.45
Fabrication	MS	MMIC	MS	CPW, MS	MS

Sizes in degree^2, MS: microstrip, CPW: coplanar wave guide.

The occupied area of the prototype excluding the IC can be calculated as $200^{\circ\wedge 2}$ by converting the physical lengths to the wavelengths, based on the substrate and the design frequency of 0.7 GHz. For [7], the CPL is 90° long which is 110 *um* in [7, Fig. 4], and the distance between two CPLs is 90 *um*, leading to the occupied area of $6627^{\circ\wedge 2}$. For [9], each CPL is 45° long which is expressed as 15.6 mm [9, Table II] where the distance between two CPLs is $L_2 + w_4 = 8.18$ mm, calculating the area as $1061^{\circ\wedge 2}$. For [10], each CPL is 40° long, and two CPLs meet at a right angle to connect a chip capacitor, calculating it as $1600^{\circ\wedge 2}$. For [12], the occupied area is written as 0.145 x 0.066 $\lambda_g{}^2$, giving $1240^{\circ\wedge 2}$. The $|S_{11}|$ bandwidth can be estimated from [12, Fig. (9)(a)] as about 18.75% (2.24 − 2.69 GHz).

On the other hand for the fabricated prototype, the 10-dB bandwidth of $|S_{11}|$ and the 15-dB isolation bandwidth of $|S_{23}|$ are 0.6-0.88 GHz (40%) and 0-0.85 GHz (121.4%), respectively, and the amplitude imbalances in the power divisions are 0.6 and 0.65 dB in $|S_{11}|$-bandwidth for the prototype. The phase imbalance is 1.2°. First of all, no conventional work for the UMs has ever demonstrated the isolation performance better than −6 dB. So, in terms of size, isolation and input matching bandwidth, the proposed UM implementation features the best performance ever recorded, considering its compactness.

VI. CONCLUSION

In this brief, a novel ultracompact and wideband UHF Marchand balun topology is introduced along with a novel IC, and accurate design formulas are given for arbitrary coupling coefficients. Even if the operating frequencies go higher than 5 GHz, the UM implementation is possible by replacing the lumped-element inductors with distributed short stubs, and if zero value of the capacitance of C_s is designed, the sizes can be reduced further. As demonstrated in Fig. 3 and the comparison data in Table III, the novel IC can give the ultracompact implementation along with excellent isolation performance and phase responses. In terms of bandwidths and size, the fabricated prototype can be considered the smallest and the best ever recorded. Therefore a big miniaturization advantage can be expected, especially for UHF applications.

REFERENCES

[1] N. Marchand, "Transmission line conversion transformers," *Electronics*, vol. 17, no. 12, pp. 142–145, Dec. 1944.

[2] H.-R. Ahn and T. Itoh, "New isolation circuits of compact impedance-transforming 3-dB baluns for theoretically perfect isolation and matching," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3892–3902, Dec. 2010.

[3] H.-R. Ahn and S. Nam, "New design formulas for impedance-transforming 3-dB Marchand baluns," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 11, pp. 2816–2823, Nov. 2011.

[4] H. J. Qian and X. Luo, "Compact 6.5–28.5 GHz on-chip balun with enhanced inband balance responses," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 12, pp. 993–995, Dec. 2016.

[5] J.-X. Xu, X. Y. Zhang, and X.-L. Zhao, "Compact LTCC balun with bandpass response based on Marchand balun," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 7, pp. 493–495, Jul. 2016.

[6] H. Jia, B. Chi, L. Kuang, and Z. Wang, "A W-band power amplifier utilizing a miniaturized Marchand balun combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 719–725, Feb. 2015.

[7] L. Xu, H. Sjöland, M. Törmänen, T. Tired, T. Pan, and X. Bai, "A miniaturized Marchand balun in CMOS with improved balance for millimeter-wave applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 1, pp. 53–55, Jan. 2014.

[8] T.-G. Ma, C.-C. Wang, and C.-H. Lai, "Miniaturized distributed Marchand balun using coupled synthesized CPWs," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 4, pp. 188–190, Apr. 2011.

[9] C.-W. Tang, W.-D. Cheng, J.-W. Wu, and Y.-C. Lin, "Design of a compact balun with three octant-wavelength coupled lines," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Anaheim, CA, USA, May 2010, pp. 109–112.

[10] K. S. Ang, Y. C. Leong, and C. H. Lee, "Analysis and design of miniaturized lumped-distributed impedance-transforming baluns," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 1009–1017, Mar. 2003.

[11] K. Nishikawa, I. Toyoda, and T. Tokumitsu, " Compact and broad-band three-dimensional MMIC balun," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 1, pp. 96–98, Jan. 1999.

[12] Y. Wang and J.-C. Lee, "A miniaturized Marchand balun model with short-end and capacitive feeding," *IEEE Access*, vol. 6, pp. 26653–26659, 2018.

[13] C. M. Montiel, "Optimization of a Marchand balun isolation circuit," in *Proc. Texas Symp. Wireless Microw. Circuits Syst. (WMCS)*, Waco, TX, USA, 2013.

[14] H.-R. Ahn and M. M. Tentzeris, "Novel generic asymmetric and symmetric equivalent circuits of 90° coupled transmission-line sections applicable to Marchand baluns," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 3, pp. 746–760, Mar. 2017.

[15] H.-R. Ahn and M. M. Tentzeris, "In-phase T-junction: Study and application to Gysel power dividers for high power-division ratios requiring no high-impedance transmission-line section," *IEEE Access*, vol. 7, pp. 18146–18154, 2019.

[16] H.-R. Ahn, *Asymmetric Passive Components in Microwave Integrated Circuits*. New York, NY, USA: Wiley, 2006.

[17] H.-R. Ahn and B. Kim, "Small wideband coupled-line ring hybrids with no restriction on coupling power," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1806–1817, Jul. 2009.

[18] H.-R. Ahn and M. M. Tentzeris, "Compact and wideband general coupled-line ring hybrids (GCRHs) for arbitrary circumferences and arbitrary power-division ratios," *IEEE Access*, vol. 7, pp. 33414–33423, 2019.