Package-Integrated, Wideband Power Dividing Networks and Antenna Arrays for 28-GHz 5G New Radio Bands

Muhammad Ali, *Graduate Student Member, IEEE*, Atom O. Watanabe, *Graduate Student Member, IEEE*, Tong-Hong Lin, Daichi Okamoto, Markondeya Raj Pulugurtha, *Senior Member, IEEE*, Manos M. Tentzeris, *Fellow, IEEE*, and Rao R. Tummala, *Life Fellow, IEEE*

***Abstract*— Package-integrated and ultrathin power dividers with footprint smaller than unit $\lambda_0{}^2$ at the operating frequency of 28-GHz 5G new radio (NR) n257 and n258 bands are presented for the first time for small-cell applications. These power dividers are also configured as antenna arrays using endfire Yagi–Uda antenna elements. Utilizing minimal matching techniques, two-, three-, and four-element antenna arrays are designed without compromising on the bandwidth of operation or electrical performance. These thin-film power dividers exhibit a cross-sectional height of 147 μm and can be implemented in the top metal layer of front-end module packages. Panel-compatible semiadditive patterning (SAP) process is utilized to realize these structures, which yields precise line space dimensions required for millimeter-wave (mm-wave) applications. This results in power dividers with low added insertion loss, low VSWR, and minimal phase difference between output ports. The added insertion loss is 25% less than similar structures reported on integrated fan-out architectures. The antenna arrays exhibit high gain and efficiency. Excellent model-to-hardware correlation is observed with multiple coupons of the same structure. Package-integrated power dividers and antenna arrays based on ultrathin laminated glass substrate represent a major step toward realizing compact mm-wave antenna-in-package for 5G small-cell applications.**

***Index Terms*— 5G and millimeter wave (mm-wave), antenna-in-package (AiP), new radio (NR), power divider, RF, semiadditive process, small cell, Yagi–Uda antenna.**

I. Introduction

HIGHLY INTEGRATED solutions for modern radios are transforming wireless communication networks to achieve higher data rates, spectral efficiency, and energy efficiency. Increased functional density of small-footprint components and modules is crucial to meet the growing demand of 5G and millimeter-wave (mm-wave) infrastructure and user equipment [1]–[3]. Package-integrated phased-array antennas and passive components, with single-chip or multichip transceiver solutions, are the key enabling technologies for the next generation of radio solutions [4]–[7]. To overcome the challenge of increased path loss with the use of 5G new radio (NR) bands such as n257 and n258 while providing Gb/s data rates with low latency, the 5G base stations and user equipment will have to rely on directed communications [8], [9]. System-level implementation challenges can be translated to IC- and package-level requirements that are vital for mm-wave 5G hardware and software codesign [10]. Some of the circuit and phased-array IC level challenges are to have reasonable spatial isolation between the links provided by beamforming, support for dual polarization and finer resolution in phase shifter. Since the antenna is the largest element in an antenna-in-package (AiP) and essentially governs its size, the antenna (or antenna array) needs to be wideband with equal length feeding lines, support dual polarization with low cross-polarization distortion, and have the tunability to support multiple beamforming and beam-steering algorithms [11], [12]. Similarly, the package needs to support heterogeneous integration of multiple RFICs for scalability, seamless routing and interconnects, high thermal efficiency, as well as multiple-functionality passive components [13].

Packaging technologies for mm-wave modules include low-temperature cofired ceramic (LTCC) [14], [15], organic

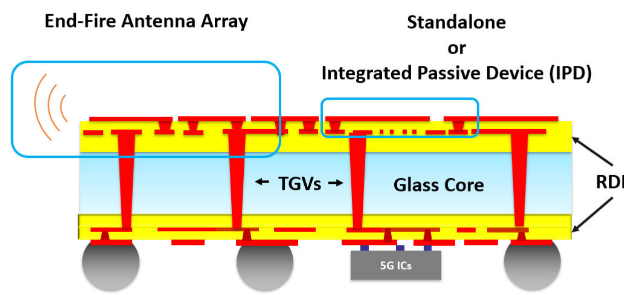

Fig. 1. Cross section of a state-of-the-art glass-based 5G module with endfire radiators for wireless communication applications.

Manuscript received June 10, 2020; accepted July 25, 2020. Date of publication August 3, 2020; date of current version September 21, 2020. This work was supported by the Industry Consortium at 3D Systems Packaging Research Center (PRC), Georgia Institute of Technology. Recommended for publication by Associate Editor W.-Y. N. Yin upon evaluation of reviewers' comments. *(Corresponding author: Muhammad Ali.)*

Muhammad Ali, Atom O. Watanabe, Tong-Hong Lin, Manos M. Tentzeris, and Rao R. Tummala are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: ali_cmi@gatech.edu; atom@gatech.edu; thlin@gatech.edu; etentze@ece.gatech.edu; rao.tummala@ece.gatech.edu).

Daichi Okamoto is with Taiyo Ink Mfg. Company Ltd., Saitama 355-0215, Japan (e-mail: okamoto.daichi@taiyoink.co.jp).

Markondeya Raj Pulugurtha is with the Department of Biomedical Engineering, Florida International University, Miami, FL 33199 USA (e-mail: mpulugur@fiu.edu).

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Digital Object Identifier 10.1109/TCPMT.2020.3013725

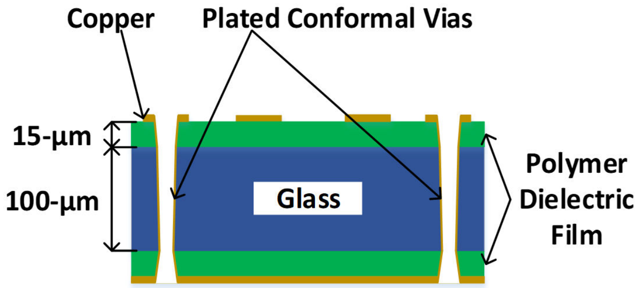


Fig. 2. Material stack-up for the demonstration of power dividers and antenna arrays.

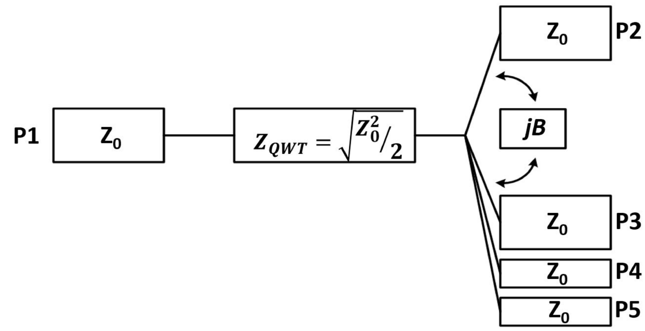


Fig. 3. Circuit schematic for designing power dividers.

laminates [4], [6], [16], [17], and fan-out wafer-level packages (FOWLPs) [18]–[20]. There are several fundamental challenges and limitations of each technology in terms of dimensions of realizable line space, precision control, density of line space, via processability, reliability, scalability, and warpage. Glass-based packaging has emerged as a competitor of these technologies to realize precision, fine-line features with silicon-like dimensional control, and tunable coefficient of thermal expansion (CTE) for various applications. In particular, mm-wave packaging applications can take advantage of fine-line features on redistribution layers (RDLs) on glass as the dimensional requirements affect the electrical performance at those frequencies. They also benefit from 3-D active components integration with shortest interconnection heights enabled by low CTE and high reliability of glass.

A cross section of a 5G AiP with endfire antennas is shown in Fig. 1. This module has heterogeneously integrated active and passive devices with high-density layers for digital routing as well as seamless interconnects and vias for low-loss RF implementation. In this article, package-integrated, ultrathin, wideband, and small-footprint (<unit $\lambda_0{}^2$) power dividers are presented for 28-GHz 5G n257 and n258 bands, which have a combined frequency range of 24.25–29.50 GHz and have a fractional bandwidth (FBW) of 19.53%. Three power divider configurations are modeled and designed: two ways, three ways, and four ways. Ultrathin glass substrate is selected as the core material onto which low-loss, thin-film polymer dielectrics are laminated. These polymer dielectrics act as fine-line RDL onto which copper is patterned precisely using semiadditive patterning (SAP) process [21]. Through-glass vias (TGVs) and via-in-via in polymer dielectrics are used to establish transmission-line structures. The power dividers are also configured as endfire antenna arrays using wideband Yagi–Uda antenna elements and can be integrated on the top metal layer of RF front-end packages with strict-footprint requirements, such as shown in Fig. 1.

II. Power Divider Design and Fabrication

A. Material Stack-Up

The material stack-up for this demonstration is shown in Fig. 2. A 15-μm epoxy film from Taiyo: Zaristo, laminated onto an AGC EN-A1 100-μm glass core, is chosen as the substrate for the power dividers. The glass substrate has a dielectric constant (Dk) of 5.4 and a loss tangent (Df) of 0.005 and Zaristo film depicts Dk of 3.2 and Df of 0.0025, characterized at 10 GHz. The desired copper thickness is set to 8 μm, which is more than five times the skin depth at the highest operating frequency of 29.50 GHz. The design rules are also set at the modeling stage and are listed in the following.

1) Critical dimension (min. width) and line space: 35 μm.
2) TGV and via-in-via diameter: 100 μm.
3) Via pitch: 450 μm.

B. Power Divider and Yagi–Uda Antenna Array Design

T-junction is the basis of transmission-line modeling of the equal-split, microstrip power dividers, as shown in Fig. 3. Alternatively, a reciprocal and matched (at all ports) power divider, commonly known as Wilkinson power divider, is frequently used as it provides isolation between output ports. For small-footprint applications, Wilkinson power divider can be disadvantageous as it requires a lumped resistor between the output legs of the power divider. Moreover, as the power division ratio is increased to more than two-way split, the Wilkinson power divider implementation becomes complex and it can require a multilayer stack-up [22]. Looking into the junction in Fig. 3, the total admittance (Y_{in}) is seen as the sum of admittance of the output legs in combination with the stored energy at the junction

$$Y_{\text{in}} = jB + \frac{1}{Z_2} + \frac{1}{Z_3} + \cdots \tag{1}$$

where jB represents the sored energy as the lumped susceptance (B) and Z_n ($n = 2, 3, 4 \ldots$) are impedances of the output legs. This susceptance in (1) can be neutralized either by discontinuity compensation or by a reactive tuning element, and it is nonzero in practice. For the demonstrated power dividers, the matching between the input and output ports is performed using a single-section quarter-wave transformer. The transformer can also aid in neutralizing jB but as the split-ratio increases, jB starts dominating and can limit the bandwidth of the structure, along with the bandwidth limitations of the impedance transformer. This was observed in the four-way power divider design in which the direct split led to slightly reduced bandwidth (18%) compared to the target. Since bandwidth is a critical performance parameter, the four-way power divider was implemented using three two-way power dividers as an alternative. Two- and three-way power dividers have reduced effects from jB and are thus more wideband than their four-way counterpart. The finalized design

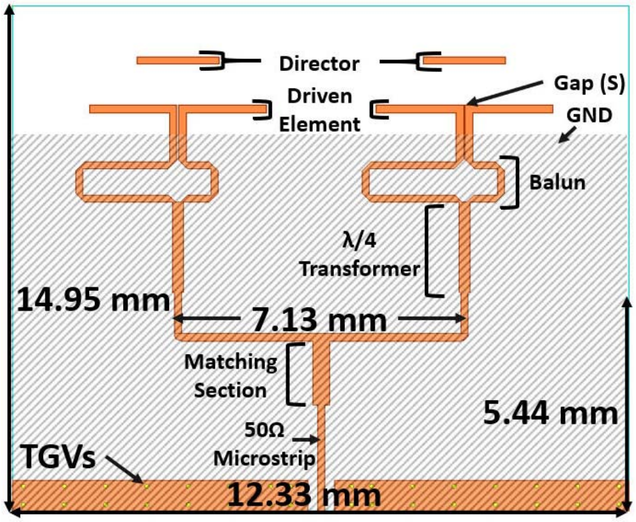


Fig. 4. Layout of 2 × 1 Yagi–Uda antenna array.

of all power dividers fulfills the bandwidth requirements and covers 24.25–29.50-GHz frequency range. Yagi–Uda antennas designed for 28-GHz 5G n257 and n258 bands with 4-dBi realized gain are then used to configure the designed power dividers as antenna arrays [23], [24].

Since the stack-up consists of three layers and the microstrip structure is selected for power dividers, it is imperative to find out the effective electrical properties to realize the transmission-line dimensions for a given impedance and electrical length. The following set of equations can be used to calculate the frequency-independent effective dielectric permittivity (ε_{rc}) of this stack-up [25], [26]:

$$\varepsilon_{rc} = \frac{|d_1| + |d_2| + |d_3|}{\left|\frac{d_1}{\varepsilon_1}\right| + \left|\frac{d_2}{\varepsilon_2}\right| + \left|\frac{d_3}{\varepsilon_3}\right|} \tag{2}$$

for $h_n + h_{n-1} + \cdots + h_1 \simeq \lambda/10$

$$d_n = \frac{K(k_n)}{K'(k_n)} - \frac{K(k_n - 1)}{K'(k_n - 1)} - \cdots - \frac{K(k_1)}{K'(k_1)}. \tag{3}$$

Generally, the value of k_n and $\frac{K()}{K'()}$ is defined as follows:

$$k_n = \frac{1}{\cosh\left(\frac{w\pi}{h_n + h_{n-1} + \ldots + h_1}\right)}, \quad \text{for } n = 1, 2, 3, \ldots \tag{4}$$

$$\frac{K(k_n)}{K'(k_n)} = \frac{1}{\pi}\ln\left(2\frac{1+\sqrt{k_n}}{1-\sqrt{k_n}}\right), \quad \text{for } 0.7 \le k_n \le 1. \tag{5}$$

ε_{rc} gives a baseline to calculate the width of the transmission lines for a certain impedance. It can also be estimated by observing the contribution of dielectric materials in this stack-up. Since Dk of the 30-μm total thickness of polymer is 3.3, Dk of the entire stack-up is estimated to be slightly less than that of glass. Full-wave electromagnetic simulators can also be used to find the dimensions of lines corresponding to required impedances. Ansoft HFSS is utilized to simulate power dividers and antenna arrays. The layout of 2 × 1 Yagi–Uda antenna array is shown as an example in Fig. 4 and its key parameters are given in Table I. As evident from the figure, TGVs are utilized to connect the top and bottom ground planes for measurements using GSG probes.

TABLE I
KEY PARAMETERS OF YAGI–UDA ANTENNA ELEMENT AND TWO-WAY POWER DIVIDER

Structure	Dimension	Value (mm)
Director	L	2
	W	0.18
Driven Element	L	4.3
	W	0.18
Balun	L	3.46
	S	0.04
λ/4 Transformer	L	2.2
	W	0.25
Matching Section	L	1.57
	W	0.4
50 Ω Microstrip	W	0.18

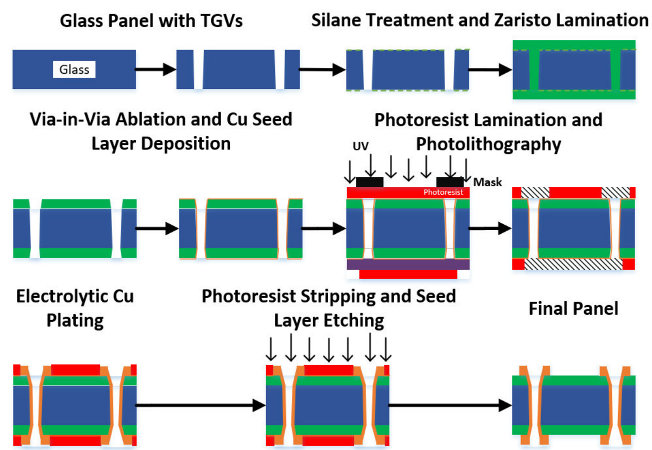


Fig. 5. Step-by-step illustration of SAP with cross sections.

C. Fabrication Process

The fabrication process utilizes the SAP process to pattern the copper structures, which has been proven superior to the conventional etching process as it provides control over the profile of deposited copper [27]–[31]. Fig. 5 shows the SAP process through schematic cross sections of each step. The process starts with a bare glass panel in which TGVs are drilled by AGC. The glass panel is then treated with silane to promote adhesion to the polymer film, and the film is laminated on the glass panel, followed by curing. Polymer lamination provides better glass handling through the rest of the process and behaves as an intermediate CTE buffer between glass and copper. Next, vias are ablated in the polymer to have through panel vias (TPV) by optimizing the via ablation conditions on a UV laser. A 200-nm-thick copper seed layer is deposited on the panel using a wet deposition process followed by lamination of dry-film negative photoresist.

Optimizing steps of SAP with experiments during fabrication is critical to obtain the desired line space dimensions. For example, desired spacing between two arms of the balun of Yagi–Uda antenna element is 40 μm. Dimensional checks are performed after the critical process to ensure tight tolerance.

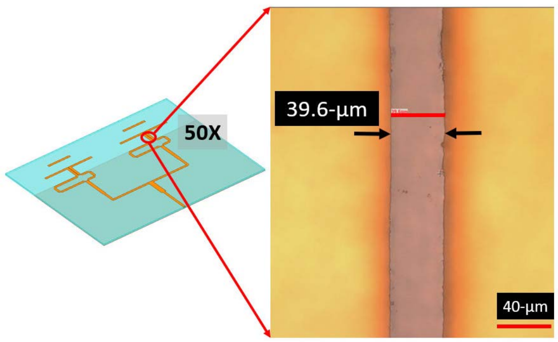
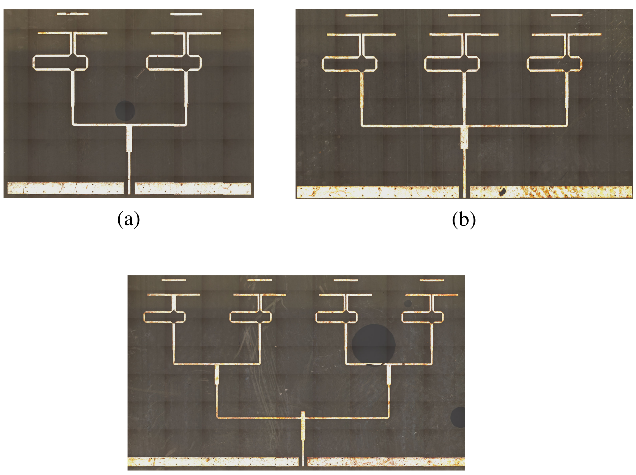


Fig. 6. Result of optimization of SAP process. Desired spacing: 40 μm. Measured: 39.6 μm.



(a) (b) (c)

Fig. 7. Fabricated coupons of Yagi–Uda antenna arrays. (a) 2×1. (b) 3×1. (c) 4×1.

As evident from Fig. 6, the measured spacing between the two arms of the balun is 39.6 μm after photolithography, photoresist development, and electrolytic plating steps. Afterward, photoresist is stripped and the seed layer is etched to obtain the desired pattern. The measured copper thickness is 8.5 $\pm$ 0.5 μm. The fabricated antenna arrays are shown in Fig. 7.

III. Characterization Results and Analysis

This section discusses the characterization results of the fabricated power dividers and corresponding antenna arrays. The return loss measurements are performed using an Anritsu vector network analyzer (VNA) in the frequency range of 20–32 GHz using ACP50 GSG probes and short-open-load-through (SOLT) calibration. For the radiation pattern measurements, 2.92-mm edge-mount connectors are soldered onto the coupons, as shown in Fig. 8. The radiation pattern measurement setup consists of a two-port VNA, two known antennas, and antenna under test (AUT). After characterizing path loss using two known antennas, one of them is replaced with AUT and its gain and radiation pattern are measured. The measurements are performed on four, three, and two coupons of 2×1, 3×1, and 4×1 antenna arrays, respectively. The measurement results are compared with the simulation results to perform a model-to-hardware correlation. Also, a dimensional analysis performed to correlate fabricated and desired dimensions and obtain electrical dimensions in terms of free-space wavelength corresponding to the center frequency of 5G NR n257 and n258 bands.

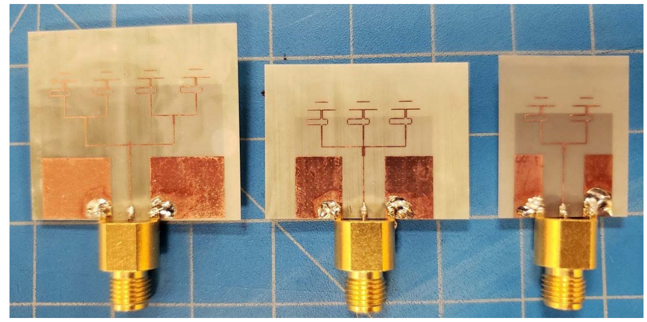
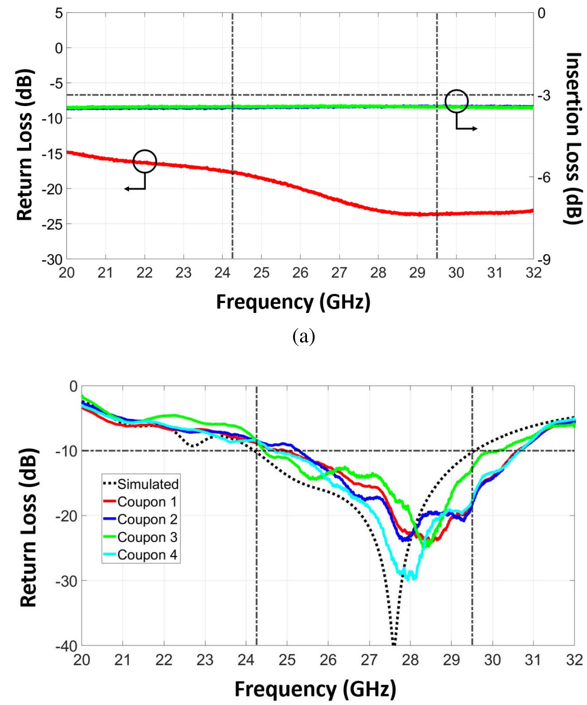


Fig. 8. Fabricated power dividers and corresponding antenna arrays (right-to-left): 2×1, 3×1, and 4×1 with soldered 2.92-mm connectors for radiation pattern measurements.



(a) (b)

Fig. 9. S-parameters. (a) Two-way power divider. (b) 2×1 Yagi–Uda antenna array.

A. Two-, Three-, and Four-Way Power Dividers

The S-parameters of two-, three-, and four-way power dividers are shown in Figs. 9(a), 10(a), and 11(a), respectively. The two-way power divider has a maximum insertion loss of 3.41 dB, the three-way power divider has a maximum insertion loss of 5.37 dB, and the four-way power divider has a maximum insertion loss of 6.88 dB. Compared with the ideal insertion loss of these power dividers, the added insertion loss is 0.4 dB for two-way power divider, 0.6 dB for three-way power divider, and 0.86 dB for four-way power divider. The in-band VSWR is less than 1.92 for the demonstrated power dividers.

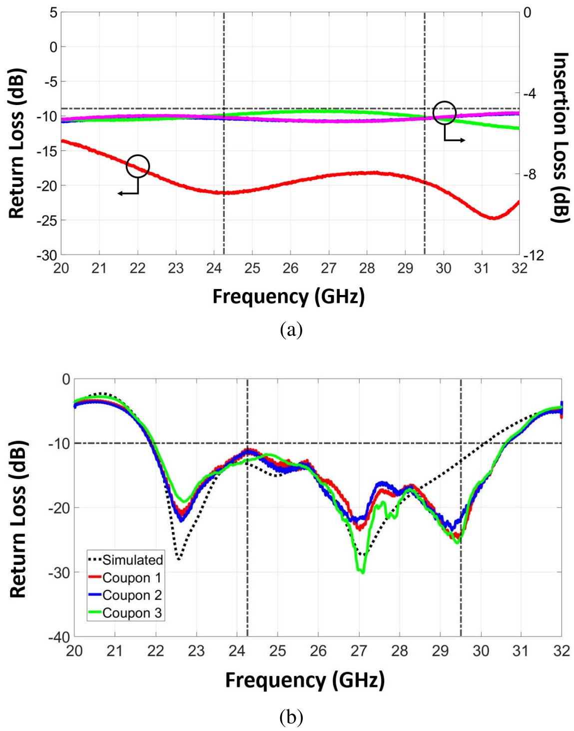


Fig. 10. S-parameters. (a) Three-way power divider. (b) 3 × 1 Yagi–Uda antenna array.

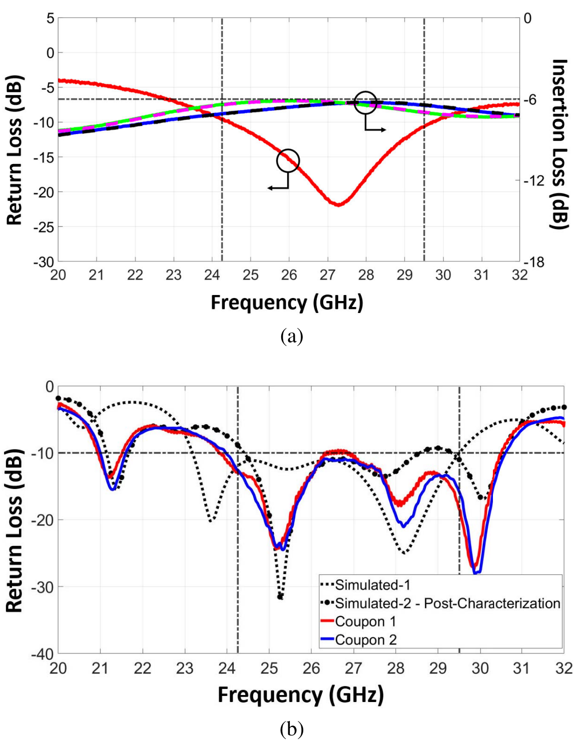


Fig. 11. S-parameters. (a) Four-way power divider. (b) 4 × 1 Yagi–Uda antenna array.

B. 2 × 1, 3 × 1, and 4 × 1 Yagi–Uda Antenna Arrays

The comparison of measured return loss of multiple coupons of 2 × 1, 3 × 1, and 4 × 1 Yagi–Uda antenna arrays with the simulation is shown in Figs. 9(b), 10(b), and 11(b), respectively. As evident from these figures, an excellent correlation is observed between the simulated and measured results, as well as between coupons of the same antenna arrays.

The model-to-hardware correlation of two-, three-, and four-way power dividers and corresponding antenna arrays is excellent as depicted in the figures. The discrepancies can be attributed to many factors in simulation, fabrication, and characterization [32]. For 4×1 antenna array, a postcharacterization simulation is performed to correlate model with hardware and understand the variation between simulation-1 and measured return loss. Mainly, the dimensions of critical features, such as gap in balun and dimensions of matching sections for all three two-way power dividers in a 4 × 1 antenna array are measured using an optical profilometer and these data are used to run a simulation in HFSS. As a result, simulation-2 captures the effects of small dimensional variations for 4 × 1 antenna array and correlates better with hardware compared with simulation-1, as shown in Fig. 11(b). The realized gain and efficiency of these antenna array structures are given in Table II. Their normalized radiation patterns are measured at 27 GHz and compared with simulation in Fig. 12. It is to be noted that the realized gain of a Yagi–Uda antenna element is 4 dBi in the 24.25–29.50-GHz frequency range.

TABLE II

REALIZED GAIN AND EFFICIENCY OF DEMONSTRATED ANTENNA ARRAYS

Structure	Realized Gain (dBi)	Efficiency
2×1 Yagi-Uda Antenna Array	6.96	80%
3×1 Yagi-Uda Antenna Array	8.24	85%
4×1 Yagi-Uda Antenna Array	9.51	82%

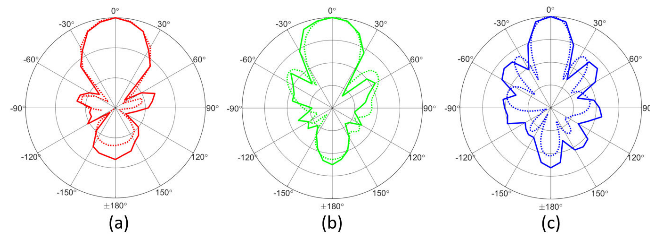


Fig. 12. Normalized measured radiation pattern of Yagi–Uda antenna arrays at 27 GHz compared with simulation (dashed line: simulated and solid line: measured). (a) 2 × 1. (b) 3 × 1. (c) 4 × 1.

TABLE III

PHYSICAL AND ELECTRICAL DIMENSIONS OF DEMONSTRATED POWER DIVIDERS AND ANTENNA ARRAYS

Structure	Physical Dimensions ($mm^2\times0.147mm$)	Electrical Dimensions ($\lambda_0^2\times0.013\lambda_0$)
Two-way Power Divider	7.13×5.44	0.64×0.49
2×1 Yagi-Uda Antenna Array	14.95×12.33	1.34×1.1
Three-way Power Divider	12.74×5.5	1.14×0.49
3×1 Yagi-Uda Antenna Array	20.6×12.5	1.85×1.12
Four-way Power Divider	21×9.7	1.88×0.87
4×1 Yagi-Uda Antenna Array	28.9×16.7	2.59×1.5

TABLE IV
COMPARISON WITH SIMILAR POWER DIVIDERS

Ref.	Structure	f_0 (GHz) & FBW	Physical Dimensions (mm^3)	Electrical Dimensions (λ_0^3)
[33]	Two-way, Tunable	28 & 7.14%	10×10×0.127	0.93×0.93×0.012
[34]	Two-way	27.5 & 91%	2.2×10.1×0.254	0.2×0.93×0.023
[35]	Four-way	28.2 & 5%	22.7×5.6×0.13	2.13×0.53×0.012
[36]	Four-way, Dual-band	28, 39 & 1.6, 5.8%	27.5×20×0.254	3.07×2.23×0.028
[18]	Two-way, InFO*	33.5 & 200%	0.96×0.36×-	0.11×0.04×-
This Work	Two-way	26.875 & 19.53%	7.13×5.4×0.147	0.64×0.49×0.013
This Work	Three-way	26.875 & 19.53%	12.7×5.5×0.147	1.14×0.49×0.013
This Work	Four-way	26.875 & 19.53%	21×9.7×0.147	1.88×0.87×0.013

* For added insertion loss comparison only. The small size of this power divider is partially due to a significantly higher design frequency.

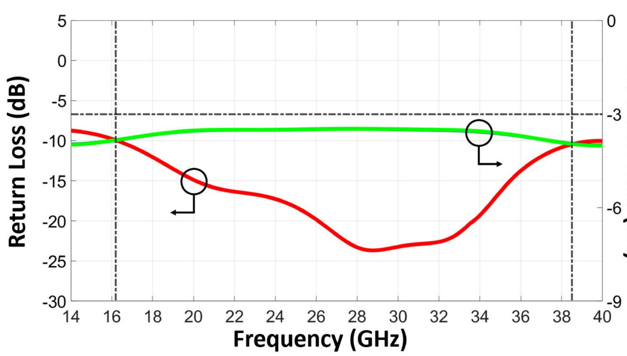


Fig. 13. Wideband S-parameters of two-way power divider.

C. Dimensional Analysis

The physical and electrical dimensions of power dividers are given in Table III. The physical dimensions are normalized with free-space wavelength (λ_0) corresponding to the center frequency (f_c) of 28-GHz 5G bands. The f_c of 24.25–29.50-GHz range is 26.875 GHz and the corresponding λ_0 is 11.16 mm. A comparison of dimensions of the demonstrated power dividers with the recent prior art is given in Table IV, in which electrical dimensions are calculated by normalizing physical dimensions by λ_0 corresponding to the band frequency. It can be observed that the demonstrated two- and three-way power dividers are smaller than unit λ_0^2. In addition, the four-way power divider has a footprint of $1.64\lambda_0^2$. All of the fabricated structures have a z-height of 147 μm. Since the power dividers are designed to be configured as antenna arrays, their footprint is governed by the physical spacing between the adjacent antenna elements. However, the footprint can be further reduced depending upon the application.

Leading-edge, thin-film, coplanar waveguide (CPW)-based ultrawideband two-way power divider is reported by TSMC on integrated fan-out (InFO) RDL [18]. This power divider depicts an insertion loss of −4.3 dB. The two-way power divider reported in this article is simulated from 14 to 40 GHz to check its wideband response. It has a −10-dB return loss FBW of 81% as shown in Fig. 13, although it was only utilized for 24.25–29.50-GHz range. Moreover, it depicts an insertion loss of −3.41 dB, which is 25% less than the power divider reported in [18]. The low added insertion loss of these power dividers can be advantageous in several component, package- and module-level applications.

IV. CONCLUSION

Package-integrated and ultrathin power dividers with footprint smaller than the unit free-space wavelength are presented for 28-GHz 5G NR n257 and n258 bands. Their design, fabrication, characterization, and analysis are discussed in detail. SAP process is optimized for the fabrication of these power-dividing structures on an ultrathin stack-up with glass substrate as a core. Moreover, the power dividers are configured as Yagi–Uda antenna arrays with up to four elements using minimal matching techniques to demonstrate the efficacy of this simple design. The characterization of power dividers and corresponding antenna arrays shows that they exhibit low added insertion loss and minimal phase shift between the output ports. An excellent agreement between the simulated and measured responses of antenna arrays is observed. The superior electrical properties of the demonstrated power dividers and antenna arrays, in combination with their small footprint, make them an ideal candidate for strict-footprint 5G and mm-wave modules.

REFERENCES

[1] V. Ilderem, "The technology underpinning 5G," *Nature Electron.*, vol. 3, no. 1, pp. 5–6, Jan. 2020, doi: 10.1038/s41928-019-0363-6.
[2] P. Mogensen *et al.*, "5G small cell optimized radio design," in *Proc. IEEE Globecom Workshops (GC Wkshps)*, Dec. 2013, pp. 111–116.
[3] A. Gupta and R. K. Jha, "A survey of 5G network: Architecture and emerging technologies," *IEEE Access*, vol. 3, pp. 1206–1232, 2015.
[4] X. Gu *et al.*, "Development, implementation, and characterization of a 64-element dual-polarized phased-array antenna module for 28-GHz high-speed data communications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2975–2984, Jul. 2019.
[5] T. Thai, S. Dalmia, J. Hagn, P. Talebbeydokhti, and Y. Tsfati, "Novel multicore PCB and substrate solutions for ultra broadband dual polarized antennas for 5G millimeter wave covering 28 GHz & 39 GHz range," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 954–959.
[6] X. Gu *et al.*, "A multilayer organic package with 64 dual-polarized antennas for 28 GHz 5G communication," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1899–1901.
[7] P. Talebbeydokhti, S. Dalmia, T. Thai, R. Sover, and S. Tal, "Ultra large area SIPs and integrated mmW antenna array module for 5G mmWave outdoor applications," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 294–299.
[8] X. Gu, B. Sadhu, D. Liu, C. Baks, and A. Valdes-Garcia, "Antenna-in-package design and module integration for millimeter-wave communication and 5G," in *Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT)*, Apr. 2018, pp. 1–2.
[9] F. Aryanfar *et al.*, "Millimeter-wave base station for mobile broadband communication," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–3.

[10] A. Valdes-Garcia *et al.*, "Circuit and antenna-in-package innovations for scaled mmWave 5G phased array modules," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–8.
[11] W. Roh *et al.*, "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: Theoretical feasibility and prototype results," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 106–113, Feb. 2014.
[12] W. Hong, K.-H. Baek, and S. Ko, "Millimeter-wave 5G antennas for smartphones: Overview and experimental demonstration," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6250–6261, Dec. 2017.
[13] H. Chu and Y.-X. Guo, "A filtering dual-polarized antenna subarray targeting for base stations in millimeter-wave 5G wireless communications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 6, pp. 964–973, Jun. 2017.
[14] B. Lee and Y. Yoon, "Low-profile, low-cost, broadband millimeter-wave antenna array for high-data-rate WPAN systems," *IEEE Antennas Wireless Propag. Lett.*, vol. 16, pp. 1957–1960, 2017.
[15] F. F. Manzillo *et al.*, "A multilayer LTCC solution for integrating 5G access point antenna modules," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2272–2283, Jul. 2016.
[16] C.-Y. Ho, M.-F. Jhong, P.-C. Pan, C.-Y. Huang, C.-C. Wang, and C.-Y. Ting, "Integrated antenna-in-package on low-cost organic substrate for millimeter-wave wireless communication applications," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, May 2017, pp. 242–247.
[17] J. Hautcoeur, K. Hettak, L. Talbi, M. Nedil, J. Shaker, and K. Wu, "A novel two-layer low-profile 23-GHz microstrip array fed by slots in an SIW for wireless backhauling applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1126–1135, Jul. 2017.
[18] C.-W. Hsu, C.-H. Tsai, J.-S. Hsieh, K.-C. Yee, C.-T. Wang, and D. Yu, "High performance chip-partitioned millimeter wave passive devices on smooth and fine pitch InFO RDL," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, May 2017, pp. 254–259.
[19] A. Hagelauer, M. Wojnowski, K. Pressel, R. Weigel, and D. Kissinger, "Integrated systems-in-package: Heterogeneous integration of millimeter-wave active circuits and passives in fan-out wafer-level packaging technologies," *IEEE Microw. Mag.*, vol. 19, no. 1, pp. 48–56, Jan. 2018.
[20] M. Wojnowski and K. Pressel, "Embedded wafer level ball grid array (eWLB) technology for high-frequency system-in-package applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–4.
[21] M. Ali *et al.*, "First demonstration of compact, ultra-thin low-pass and bandpass filters for 5G small-cell applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 12, pp. 1110–1112, Dec. 2018.
[22] D. M. Pozar, *Microwave Engineering*. Hoboken, NJ, USA: Wiley, 2005. [Online]. Available: https://books.google.com/books?id=LwisngEACAAJ
[23] M. Ali, A. Watanabe, T.-H. Lin, M. R. Pulugurtha, M. M. Tentzeris, and R. R. Tummala, "3D glass package-integrated, high-performance power dividing networks for 5G broadband antennas," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 960–967.
[24] A. Watanabe *et al.*, "Leading-edge and ultra-thin 3D glass-polymer 5G modules with seamless antenna-to-transceiver signal transmissions," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 2026–2031.
[25] M. Kobayashi, "A dispersion formula satisfying recent requirements in microstrip CAD," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 8, pp. 1246–1250, Aug. 1988.
[26] E. O. Hammerstad, "Equations for microstrip circuit design," in *Proc. 5th Eur. Microw. Conf.*, Oct. 1975, pp. 268–272.
[27] P. M. Raj *et al.*, "'Zero-undercut' semi-additive copper patterning-a breakthrough for ultrafine-line RDL lithographic structures and precision RF thinfilm passives," in *Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 402–405.
[28] H. Lu *et al.*, "Design, modeling, fabrication and characterization of 2–5-μm redistribution layer traces by advanced semiadditive processes on low-cost panel-based glass interposers," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 6, pp. 959–967, Jun. 2016.
[29] A. O. Watanabe *et al.*, "First demonstration of 28 GHz and 39 GHz transmission lines and antennas on glass substrates for 5G modules," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, May 2017, pp. 236–241.
[30] M. Ali *et al.*, "Miniaturized high-performance filters for 5G small-cell applications," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 1068–1075.
[31] M. Ali, A. Watanabe, T.-H. Lin, M. Tentzeris, R. Tummala, and P. M. Raj, "Ultra-wideband, glass package-integrated power dividers for 5G and mm-wave applications," in *Proc. IEEE Int. Symp. Antennas Propag. USNC-URSI Radio Sci. Meeting*, Jul. 2019, pp. 863–864.
[32] E. Usta and N. T. Tokan, "Effects of surface finish material on millimeter-wave antenna performance," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 5, pp. 815–821, May 2019.
[33] E. Al Abbas and A. Abbosh, "Millimeter wave tunable power divider using modified Wilkinson design," in *Proc. IEEE 2nd Austral. Microw. Symp. (AMS)*, Feb. 2016, pp. 3–4.
[34] P. Wu, Y. Zhang, and Q. Zhang, "A novel wideband Wilkinson divider using parallel branch lines," *Microw. Opt. Technol. Lett.*, vol. 53, no. 4, pp. 781–783, Apr. 2011, doi: 10.1002/mop.25833.
[35] A. T. Alreshaid, O. Hammi, M. S. Sharawi, and K. Sarabandi, "A compact millimeter-wave slot antenna array for 5G standards," in *Proc. IEEE 4th Asia–Pacific Conf. Antennas Propag. (APCAP)*, Jun. 2015, pp. 84–85.
[36] N. Ashraf, O. Haraz, M. A. Ashraf, and S. Alshebeili, "28/38-GHz dual-band millimeter wave SIW array antenna with EBG structures for 5G applications," in *Proc. Int. Conf. Inf. Commun. Technol. Res. (ICTRC)*, May 2015, pp. 5–8.

Muhammad Ali (Graduate Student Member, IEEE) received the bachelor's degree in electrical engineering from the National University of Science and Technology (NUST), Rawalpindi, Pakistan, in 2013, and the M.Sc. degree in electrical and computer engineering (ECE) from the Georgia Institute of Technology, Atlanta, GA, USA, in 2017. He is currently pursuing the Ph.D. degree in ECE with the 3D Systems Packaging Research Center (PRC), Georgia Institute of Technology, advised by Prof. R. Tummala.

As a Graduate Research Assistant (GRA) at GT-PRC, he has been working on modeling, design, fabrication, and characterization of miniaturized, high-performance passive components for 5G and mm-wave applications on ultrathin glass. His research interests include RF/millimeter-wave passive component design, electronic systems and packaging, and system performance analysis techniques.

Mr. Ali was a recipient of the Intel Best Student Paper Award at the IEEE 68th Electronic Components and Technology Conference (ECTC), held May 29–June 1, 2018, in San Diego, CA, USA, and the prestigious Fulbright Scholarship. He received the ECTC Student Travel Award sponsored by the IEEE Electronics Packaging Society (EPS) in 2019.

Atom O. Watanabe (Graduate Student Member, IEEE) received the B.Eng. degree in applied physics and physico-informatics from Keio University, Tokyo, Japan, in 2015. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the 3-D Systems Packaging Research Center, Georgia Institute of Technology, Atlanta, GA, USA, under the guidance of Prof. R. R. Tummala and Prof. M. Swaminathan.

In 2013, he joined the Finding Nano program organized by the Technical University of Munich, Munich, Germany. As a Graduate Research Assistant in the RF/5G Glass Interposer Program, Georgia Tech PRC, he is involved in the design and demonstration of high-performance and ultrathin antenna-integrated 3-D glass-based millimeter-wave (mm-wave) packages. His current research interests include RF/mm-wave system-on-package technology with electrical designs and processes, antenna integration, and signal and power integrity.

Tong-Hong Lin received the B.S.E.E. and M.S. degrees in communication engineering from National Taiwan University, Taipei, Taiwan, in 2011 and 2013, respectively, and the M.S. degree in computational science and engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2020, where he is currently pursuing the Ph.D. degree in electrical and computer engineering.

He is currently a Research Assistant with the ATHENA Group and the 3D Systems Packaging Research Center, Georgia Institute of Technology. His current research interests include characterization of inkjet printing and 3-D printing material properties and fabrication processes, application of additive manufacturing technologies to wearable and flexible electronics, RF energy harvesting systems, wireless power transfer systems, wireless sensing networks, antenna-in-package design, RF/millimeter-wave packaging design, 5G system-on-package modules, and glass packaging design.

Mr. Lin was a recipient of the Student Travel Award of the 2018 IEEE Electronic Components and Technology Conference (ECTC).

Daichi Okamoto received the M.S. degree in analytic chemistry from the Toyohashi University of Technology, Toyohashi, Japan, in 2007.

He joined Taiyo Ink Mfg. Company Ltd., Saitama, Japan, where he had been engaged in the development and application of solder resist for integrated circuit packaging substrate since 2007. In 2015, he was dispatched to Cupertino, CA, USA, as a Marketing Manager to promote Taiyo's products. From 2017 to 2019, he was with the 3D Systems Packaging Research Center, Georgia Institute of Technology, Atlanta, GA, USA, as a Visiting Engineer, where he was involved in the 2.5-D glass interposer and RF/5G packaging program.

Markondeya Raj Pulugurtha (Senior Member, IEEE) received the B.S. degree from IIT Kanpur, Kanpur, India, in 1993, the M.E. degree from the Indian Institute of Science, Bengaluru, India, in 1995, and the Ph.D. degree from Rutgers University, New Brunswick, NJ, USA, in 1999.

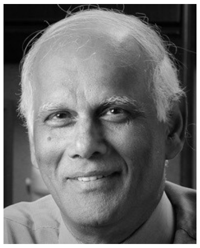
He is currently an Associate Professor of biomedical engineering and ECE (electrical and computer engineering), Florida International University, Miami, FL, USA. He is also an Adjunct Professor with the Department of Electrical and Computer Engineering and the Packaging Research Center, Georgia Institute of Technology, Atlanta, GA, USA. His expertise is in packaging of electronic and bioelectronic systems, power-supply and wireless component integration in flex and rigid packages, and biocompatible and hermetic packaging with high-density feedthroughs. He co-lead several technical thrusts in electronic packaging, working with the whole electronic ecosystem, which includes semiconductor, packaging and material, tool, and end-user companies. He is widely recognized for his contributions in integrated passive components and technology roadmapping, component integration for bioelectronic, power, and RF modules, and also for promoting the role of nanomaterials and nanostructures for electronics packaging applications, as evident through his several industry partnerships, invited presentations, publications, and awards. His research led to 330 publications, which include 20 book chapters. He received eight patents with several other provisional patents and invention disclosures. He has been a Research Faculty Member at GT-PRC for 19 years, where he mentored more than 25 M.S. and Ph.D. students.

Dr. Pulugurtha's research led to more than 25 best paper awards. He is also the IEEE NTC Distinguished Lecturer in 2020, an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY and the *IEEE Nanotechnology Magazine* and the Co-Chair of the IEEE Nanopackaging Technical Committee. He has been instrumental in forming the "Nanopackaging" and "Heterogeneous Integration" technical sessions at various IEEE conferences. He has been actively involved with the Power Sources Manufacturers Association (PSMA) and takes a proactive role in shaping up power electronics sessions at APEC and PEIM conferences. He serves as a reviewer for about six to eight journal articles every month. He is also an STEM Ambassador and frequently offers nanoscience and nanotechnology demonstrations at local schools and hosts K-12 field trips.

Manos M. Tentzeris (Fellow, IEEE) received the Diploma degree *(magna cum laude)* in electrical and computer engineering from the National Technical University of Athens, Athens, Greece, in 1992, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of Michigan, Ann Arbor, MI, USA, in 1993 and 1998, respectively.

He was a Visiting Professor with the Technical University of Munich, Munich, Germany, in 2002, GTRI-Ireland, Athlone, Ireland, in 2009, LAAS-CNRS, Toulouse, France, in 2010, and Friedrich Alexander University, Erlangen, Germany, in 2019. He has served as the Head of the GTECE Electromagnetics Technical Interest Group, as the Georgia Electronic Design Center Associate Director of RFID/Sensors research, as the Georgia Institute of Technology NSF-Packaging Research Center Associate Director of RF Research, and as the RF Alliance Leader. He is currently a Ken Byers Professor in flexible electronics with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, where he heads the ATHENA Research Group (20 researchers). He has helped develop academic programs in 3-D/inkjet-printed RF electronics and modules, flexible electronics, origami and morphing electromagnetics, highly integrated/multilayer packaging for RF and wireless applications using ceramic and organic flexible materials, paper-based RFID's and sensors, wireless sensors and biosensors, wearable electronics, "Green" electronics, energy harvesting and wireless power transfer, and nanotechnology applications in RF, microwave MEMs, and SOP-integrated (UWB, multiband, millimeter wave, and conformal) antennas. He has authored more than 650 800 papers in refereed journals and conference proceedings, 65 books, and 265 book chapters.

Dr. Tentzeris is a member of the URSI-Commission D, the MTT-15 Committee, and the Technical Chamber of Greece, an Associate Member of EuMA, and a Fellow of the Electromagnetic Academy. He was a recipient/co-recipient of the 2019 Humboldt Re-search Prize, the 2017 Georgia Institute of Technology Outstanding Achievement in Research Program Development Award, the 2016 Bell Labs Award Competition 3rd Prize, the 2015 IET Microwaves, Antennas, and Propagation Premium Award, the 2014 Georgia Institute of Technology ECE Distinguished Faculty Achievement Award, the 2014 IEEE RFID-TA Best Student Paper Award, the 2013 IET Microwaves, Antennas and Propagation Premium Award, the 2012 FiDiPro Award in Finland, the iCMG Architecture Award of Excellence, the 2010 IEEE Antennas and Propagation Society Piergiorgio L. E. Uslenghi Letters Prize Paper Award, the 2011 International Workshop on Structural Health Monitoring Best Student Paper Award, the 2010 Georgia Institute of Technology Senior Faculty Outstanding Undergraduate Research Mentor Award, the 2009 IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGIES Best Paper Award, the 2009 E. T. S. Walton Award from the Irish Science Foundation, the 2007 IEEE AP-S Symposium Best Student Paper Award, the 2007 IEEE MTT-S IMS Third Best Student Paper Award, the 2007 ISAP 2007 Poster Presentation Award, the 2006 IEEE MTT-S Outstanding Young Engineer Award, the 2006 Asia–Pacific Microwave Conference Award, the 2004 IEEE TRANSACTIONS ON ADVANCED PACKAGING Commendable Paper Award, the 2003 NASA Godfrey "Art" Anzic Collaborative Distinguished Publication Award, the 2003 IBC International Educator of the Year Award, the 2003 IEEE CPMT Outstanding Young Engineer Award, the 2002 International Conference on Microwave and Millimeter-Wave Technology Best Paper Award, Beijing, China, the 2002 Georgia Institute of Technology–ECE Outstanding Junior Faculty Award, the 2001 ACES Conference Best Paper Award, the 2000 NSF CAREER Award, and the 1997 Best Paper Award of the International Hybrid Microelectronics and Packaging Society. He was the TPC Chair of the IEEE MTT-S IMS 2008 Symposium and the Chair of the 2005 IEEE CEM-TD Workshop. He is also the Vice-Chair of the RF Technical Committee (TC16) of the IEEE CPMT Society. He is also the Founder and the Chair of the RFID Technical Committee (TC24) of the IEEE MTT-S and the Secretary/Treasurer of the IEEE C-RFID. He is also an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON ADVANCED PACKAGING, and the *International Journal on Antennas and Propagation*. He has given more than 100 invited talks to various universities and companies all over the world. He has served as one of the IEEE MTT-S Distinguished Microwave Lecturers from 2010 to 2012 and is one of the IEEE CRFID Distinguished Lecturers.



Rao R. Tummala (Life Fellow, IEEE) was an IBM Fellow and the Director of the Advanced Packaging Lab (APTL), Wheeling, IL, USA, pioneering such major technologies as the industry's first plasma display in the 1970s and, the first and next two generations of 100-chip MCM package integration, now called chiplet MCMs, in the 1980s for servers, mainframes, and supercomputers in 1993. He is currently a Distinguished and Endowed Chair Professor and the Director Emeritus at Georgia Tech, Atlanta, GA, USA. He is well known as an industrial technologist, a technology pioneer, and an educator. He is the father of system-on-package (SOP) concept versus system-on-chip (SOC.) As an educator, he was instrumental in setting up the largest and most comprehensive academic center funded by NSF as the first and only NSF Engineering Research Center in Electronic Systems Packaging at Georgia Tech. Such a center, under his leadership, pioneered an integrated approach to research, education, and global industry collaborations. It involved about 30 academic and full-time research faculty, 200 Ph.D. and M.S. students, and 50–70 industry and academic collaborators from USA, Europe, Japan, South Korea, India, and Taiwan. It educated thousands of engineers in packaging in classrooms and labs and produced more than 1000 engineers with Ph.D., M.S., and B.S. degrees. He has published about 800 technical articles and invented technologies that resulted in over 110 patents and inventions. He wrote the first modern handbook in packaging *Microelectronics Packaging Handbook* (McGraw-Hill, 1988), then first undergrad textbook *Fundamentals of Microsystem Packaging* (2001), the first book introducing the concept of SOP *Introduction to System-on-Package* (2006), and *Fundamentals of Device and Systems Packaging* (2020, Second Edition).

Dr. Tummala is a member of the National Academy of Engineering (NAE) and International Microelectronics Assembly and Packaging Society (IMAPS), a Fellow of the American Ceramic Society, and the President of the IEEE CPMT and IMAPS Societies. He received more than 50 industry, academic and professional society awards, including 12 invention and four corporate awards from IBM, the IEEE Award David Sarnoff Award for Industry's First MCM in 1991, the ASM-International: Engineering Materials Achievement Award for LTCC in 1992, the IEEE CPMT: Sustained Technical Achievement Award in 1992, the European Electronic Materials Award from DVM in 1995, the International Microelectronic and Packaging Society's (IMAPS): Dan Hughes Award in 1997, the American Ceramic Society's John Jeppson Award in 1998, IMAPS': John A. Wagnon's Award in 1998, named by the U.S. News and World Report as one of the 50 Stars in USA for U.S. competitiveness in 1999, the Total Excellence in Manufacturing Award from ASE in 2000, the Educator of the Year for Excellence in Teaching, Research, and Innovation in Electronics from the India–America Cultural Association in 2002, and the Techno-visionary Award from the Semiconductor Industry Association of India in 2010. He is also a Distinguished Alumni of the Indian Institute of Science, Bengaluru, India, in 2000, the University of Illinois in 1988, and a Distinguished Faculty of Georgia Tech in 2002. He has been a consultant and advisor to many of Fortune 500 semiconductor and systems companies.