Flexible/Conformal Inkjet-Printed 3-D "Ramp" Interconnects for 5G/mmWave System-on-Package Designs and Wearable Applications

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***Abstract*— This article presents the first and most comprehensive design, fabrication, and reliability evaluation of the electrical and mechanical performance of fully inkjet-printed 3-D "ramp" interconnects. Inkjet-printed interconnects feature superior RF performance and better mechanical reliability for heterogeneous integration for 5G mmWave flexible electronics packaging. The packaged systems are required to survive various flexing conditions over a large number of cyclic bending for conformal applications. In this work, ramp interconnects are designed with excellent and reliable performance for flexible packaging over the 20–40-GHz frequency band. A test vehicle of a monolithic microwave integrated circuit (MMIC) attenuator die placed in the middle of two microstrip lines is used, where ramp interconnects are fabricated by inkjet printing SU8 dielectric ink to form ramp base and inkjet printing silver nanoparticle (SNP) ink for conductive interconnects to build the connection between the die and microstrip lines. The fabricated sample exhibits a superior S_{21} performance with less than 1.16-dB insertion loss per interconnect throughout the whole operation range from 20 to 40 GHz. Monotonic bending tests are conducted over mandrels of various radii ranging from 50 to 10 mm, and the designed ramp interconnects are able to maintain robust transmission with a minimum variation of less than 0.15-dB insertion loss per interconnect. Moreover, the fabricated samples are able to survive over 20 000 times of cyclic bending tests over the mandrel of 10-mm radius, with less than 0.2-dB additional loss from each interconnect. The proposed design takes advantage of a low-cost, on-demand additive manufacturing method by selectively depositing SU8 ink layer by layer with varying dimensions to enable rugged ramp structures for curved mounting platforms. The results reported in this article could enable rapid production of high-performance and reliable flexible system-on-package (SoP) and multichip module (MCM) designs and build the foundation of next-generation 5G mmWave flexible hybrid electronics (FHE) technologies for various applications.**

***Index Terms*— 5G, additive manufacturing, electronics packaging, flexible electronics, flexible interconnects, inkjet printing, reliability.**

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I. Introduction

THE recent strides in 5G mmWave technologies hold immense promise for the development of next-generation data-centric Internet-of-Things (IoT) systems, expansive smart city infrastructures, and health monitoring wearable electronics [1], featuring broadband operation and high-speed data transmission. Consequently, there is a growing need for future system-on-package (SoP) designs that demand reliable performance across a wide bandwidth, minimum parasitic losses, high volumetric utilization to enable multifunctional compact modules [2], and robust mechanical flexibility for seamless conformity to various conformal platforms [3]. However, successful realization of these designs relies heavily on the efficiency of various interconnects among different devices within multilayered and multimaterial topologies. Conventional interconnections in the mmWave spectrum often rely on thermosonic ribbon or wirebonds to establish connections between ICs and the host packaging substrate or printed circuit board (PCB) and often exhibit limitations such as increased loop length, elevated parasitic inductance at high frequencies, and notable discontinuities [4]. They can inadvertently cause radiation losses due to the arching nature of bond wires [5]. In contrast, additively manufactured interconnects offer a more robust, planar, and adaptable structure, resulting in enhanced RF performance, especially in challenging configurations. The utilization of additive manufacturing technologies such as inkjet printing and 3-D printing enables on-demand packaging capabilities with a variety of materials, facilitating the creation of diverse customized components that can be swiftly assembled in a heterogeneous topology. Furthermore, as the operational frequencies of devices increase, the deployment of numerous small cells is required to minimize high path loss and optimize communication channels. The utilization of additive manufacturing techniques can drastically reduce the cost and expedite the implementation of 5G networks.

The early implementation of additively manufactured interconnect structures using inkjet printing can be found in [6], where a system-in-package design was integrated through printed interconnections, printed insulating layers, and printed conductive traces [6]. The first inkjet-printed "ramp" interconnect structure was introduced and characterized in 2016 [7]. The sloped "ramp" interconnect structures have found practical applications in MMIC integration, showcasing a loss of 0.57 dB/mm in Ka-band low-noise amplifier (LNA)

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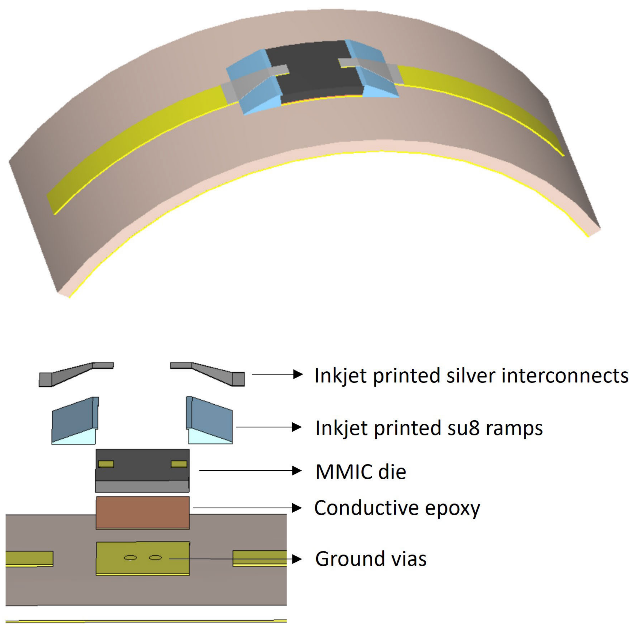

Fig. 1. Demonstration of flexible inkjet-printed 3-D "ramp" interconnects.

setups. The discrete ramp-interconnect-enabled packaging technique allows direct MMIC placement on the substrate without the need for costly substrate-damaging cavity machining. A fully additively manufactured RF front-end multichip module (MCM) module was reported in [8], where the inkjet-printed interconnects featured an average of 0.5-dB insertion loss over 10–40 GHz and demonstrated 3.3-dB peak improvement in insertion loss compared with wire bonds, suggesting superior RF performance in additively manufactured interconnects. Recent advancements in this area focused on exploring aerosol jet printing to deposit nanocomposite films, such as barium titanate, for fabricating capacitors used in dc bypasses [9]. This technique shows similar packaging loss (0.55 dB/mm at 15 GHz) to previously reported methods [10]. Similar "ramp" interconnect designs were also seen in [12], [13], [14], and [15], covering various frequency bands between 20 and 85 GHz, with ultralow loss varying from 0.2 to 1.1 dB. Aerosol jet printing can provide enhanced resolution capabilities in comparison to inkjet printing, but it operates at a higher cost and uses only a limited number of printing nozzles. This contrasts with commercial inkjet printheads, which offer thousands of printing nozzles, thus rendering aerosol jet printing less suitable for large-scale production environments. While extensive research has explored the integration of additively manufactured interconnects, the existing body of work has not specifically addressed the flexibility inherent in the "ramp" interconnect configuration. Therefore, there is a need for further investigation of the fabrication process, as well as the evaluation of the reliability of this particular additively manufactured interconnect design across diverse flexing conditions.

This article presents the design, fabrication, and reliability evaluation of inkjet-printed ramp interconnects for flexible packaging applications over 20–40 GHz, covering the 5G mmWave frequency band. To demonstrate and characterize RF performance, wideband attenuator dies are used as test vehicles to interface with two microstrip lines by inkjet printing SU8 as dielectric ramp base and silver nanoparticle (SNP) ink as conductive traces, as shown in Fig. 1. The substrate used for fabrication is Rogers 3003 with 0.13-mm thickness, to ensure enough flexibility for the samples. The functional maximum bending radius of the inkjet-printed ramp interconnects is evaluated through monotonic bending tests over mandrels of various radii ranging from 5 to 50 mm to assess their performance on different conformal platforms. In addition, the fabricated samples are subjected to 20 000 cyclic bending tests over a mandrel of 10-mm radius to evaluate the fatigue mechanism in insertion loss. Furthermore, by selectively depositing SU8 dielectric ink layer by layer with varying dimensions, the rugged ramp base for the interconnects can be adjusted in length and slope to fit the needs of different components on curved surfaces, and the SU8 encapsulation can provide additional protection for the interconnects to survive more extreme flexing conditions. To the best of the authors' knowledge, this article presents for the first time that in the mmWave regime, the inkjet-printed ramp interconnects have been thoroughly characterized and evaluated for reliability in both electrical and mechanical performance, which could potentially provide guidelines and build the foundations for future flexible SoP and MCM designs.

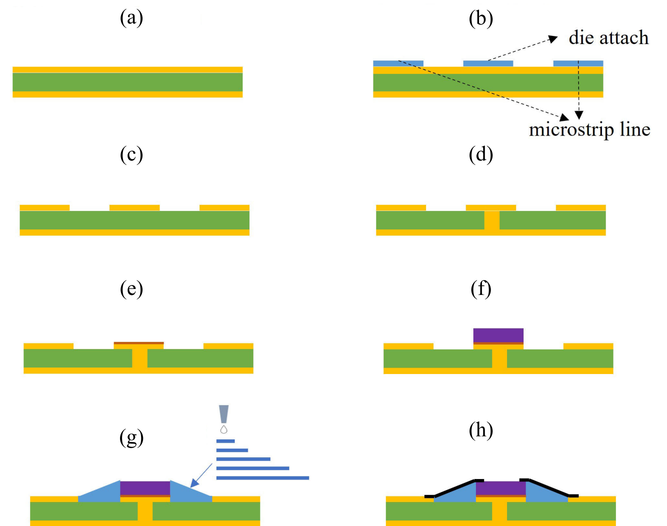

Fig. 2. Fabrication process of inkjet-printed 3-D "ramp" interconnects. (a) Prepare substrate. (b) Inkjet print SU8. (c) Etch substrate. (d) Make vias. (e) Apply epoxy. (f) Attach component. (g) Inkjet print SU8. (h) Inkjet print silver.

II. Sample Preparation

A. Fabrication Process

The ramp interconnect samples used for the reliability tests consist of a microstrip line and a 0-dB fixed attenuator die KAT-0-D+ from Mini-Circuits. The MMIC die has the dimensions of 700 μm in width, 750 μm in length, and 100 μm in thickness. The microstrip line is aimed to help with measurements and evaluation of bending over various radii. Rogers 3003 material with 0.13-mm dielectric thickness and 17-μm copper thickness was chosen to ensure enough flexibility for bending tests. The fabrication process is demonstrated in Fig. 2. A MicroChem SU-8 polymer-based dielectric ink was first deposited onto the substrate using Fuji Dimatix 2850 inkjet printer to create the microstrip line pattern with a

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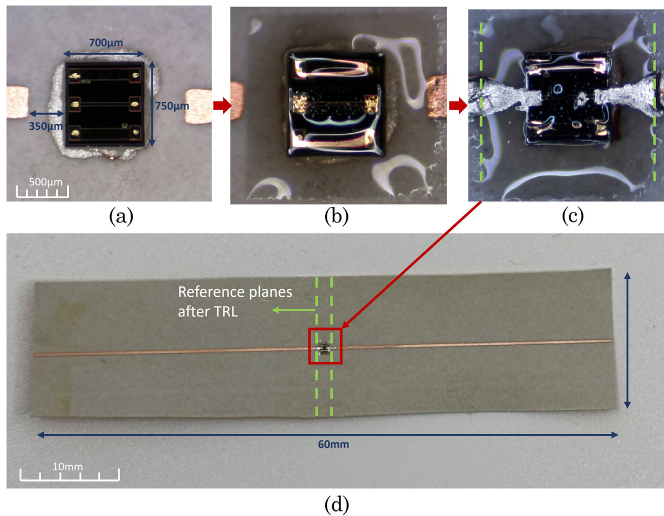

Fig. 3. Prototype images of inkjet-printed ramp interconnects interfacing an MMIC GaAs attenuator die. (a) Die attachment. (b) Inkjet-printed SU8 ramps. (c) Inkjet-printed SNP interconnects. (d) Fabricated sample.

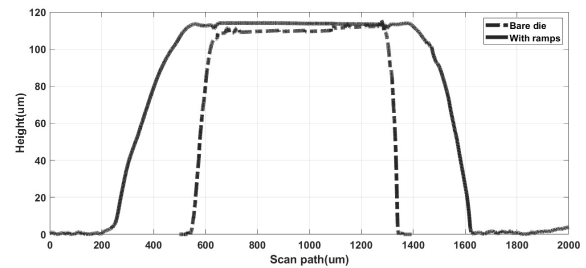

Fig. 4. Comparison of profilometer scan of the MMIC die with and without inkjet-printed 3-D interconnects.

TABLE I

MEASURED CONDUCTIVITY AND INSERTION LOSS OF SNP INK [11]

Printed Layers	3	6	9
Ink Thickness (µm)	6.13	9.52	14.82
Conductivity ($\times 10^7$ S)	1.808	4.44	7.59
Insertion Loss 20-40GHz (dB/mm)	0.074– 0.130	0.059– 0.101	0.048– 0.080

center gap of 1400 μm and a center pad of 700 $\times$ 750 μm, which was used for die attachment in the following steps. The SU8 ink was then cured by ultraviolet (UV) exposure, and the uncovered copper was etched off using ferric chloride to reveal the printed pattern. Ground vias were made by drilling through the center pad and filling the drilled hole with LPKF silver paste, followed by 30-min thermal curing under 160 °C in the oven. Once the base substrate with the microstrip line with die attach was ready, the attenuator die was carefully placed onto the center pad using a pick-and-place tool, and silver epoxy was used to allow for a reliable attachment between the die and the pad.

To fabricate the ramp interconnects, 12 layers of SU8 ink were inkjet-printed in a novel "staircase" fashion with varying lengths, from 350 to 100 μm with every two layers decreasing by 50 μm, to form a rugged and smooth ramp transition from the edge of the microstrip line to the edge of the die, as shown in step 7 from Fig. 2. For each layer of SU8 for the ramp, the printing pattern is designed to be a square shape covering the whole MMIC, with a slot opening for the RF in/out bonding pads only, as shown in Fig. 3(b). This step aims to fortify the MMIC attachment while ensuring the ramp base's durability to withstand bending across curved surfaces. The end of the ramp is also extended 20 μm to the edge of the die and 30 μm to the edge of the microstrip line to help create a seamless exterior for the interconnects. The selected effective length of the ramp interconnects along the substrate is 400 μm, a choice made to align with the typical length of conventional bond wires [18] and established practices in additively manufactured interconnects found in the existing literature [8], [13] that operate in the same frequency band. The printed SU8 "ramp" was first baked with 60 °C–120 °C ramp over 10 min, followed by a 250-mJ/cm^2 exposure of 365-nm UV light and a 100 °C bake for 7 min. The baking cycle was aimed to improve the adhesion and mechanical strength of the SU8 ramp. Afterward, a 2-min UV ozone (UVO) treatment was performed to improve surface wetting and ink adhesion for silver. For each interconnect, a short tapered line of 400 μm in length was inkjet-printed onto the ramp using SNP ink EMD5370 from Sun Chemical. The tapered line connects the microstrip line with 320-μm width to the RF input/output pad of the attenuator die with 125-μm width to help achieve better impedance matching. Three layers of SNP ink were deposited in total to ensure good electrical connection and ink coverage. The printed SNP ink was then dried and half-sintered under 90 °C for 10 min. Finally, UV sintering of 830 J was applied using Xenon X-100 to fully sinter the printed silver ink. The fabricated prototype is shown in Fig. 3. Traditional thermal sintering of 130 °C–160 °C for 1 h can be an alternative sintering method to achieve higher conductivity. UV sintering was used in this article to show the potential application of the proposed fabrication process onto other flexible substrates that cannot stand high temperatures, e.g., 3-D-printed flexible polymer materials [19].

B. Material Characterization

The SU8 dielectric ink has been used to pattern 3-D features ranging from tens to hundreds of microns in thickness. Once deposited and cured, this material exhibits a relative permittivity of approximately 3.2 and a loss tangent of 0.04 at 24.5 GHz [16]. The profile of the printed ramp base can be measured using a profilometer, which is shown in Fig. 4. It can be seen that by printing 12 layers of SU8 ink with progressively varying dimensions, a very smooth and uniform ramp base can be formed for the interconnects. The slope angle of the ramp is around 16°, decided by the thickness of the MMIC (100 μm) and the length of the ramp base (350 μm), which is adjustable by changing the number of the printed SU8 layers and the dimensions of each layer. In addition, to understand the electrical properties of the SNP ink, different metallization thickness was previously characterized and measured over SU8 buffer layers to evaluate conductivity [11]. The results are recorded in Table I. Three layers of silver ink

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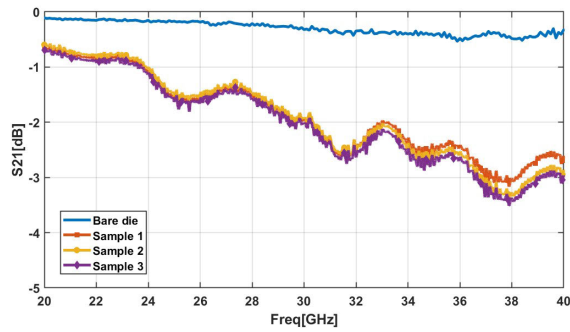


Fig. 5. Measured S_{21} results for inkjet-printed ramp interconnects with a 0-dB GaAs attenuator die.

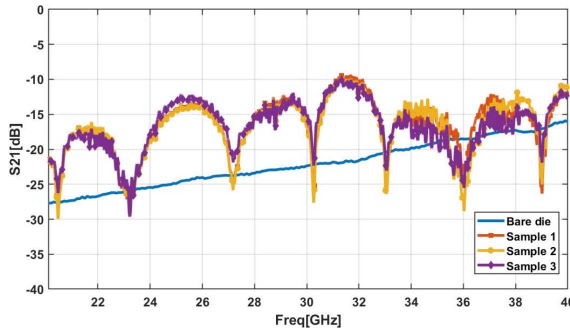


Fig. 6. Measured S_{11} results for inkjet-printed ramp interconnects with a 0-dB GaAs attenuator die.

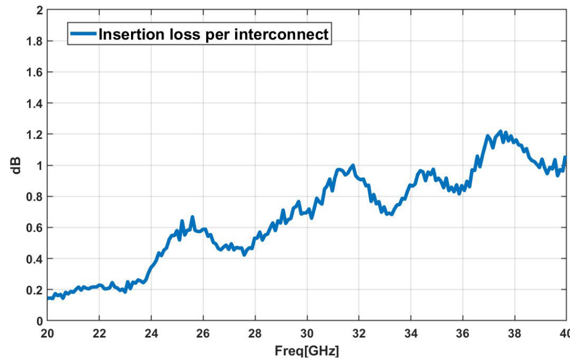
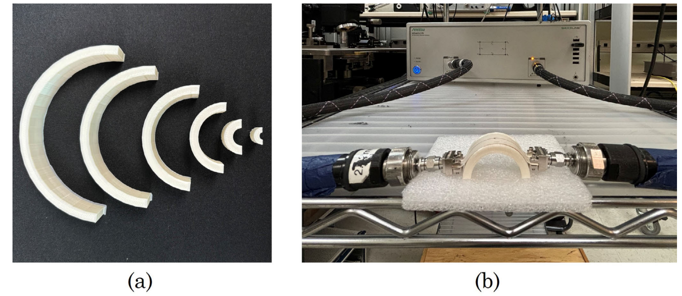


Fig. 7. Average de-embedded insertion loss for each inkjet-printed ramp interconnect.

are printed in this research to avoid the spreading of the ink during printing and allow faster iterations of the fabrication.

C. RF Characterization of Ramp Interconnects

To characterize the RF performance of the fabricated ramp interconnects, three samples were prepared and measured. The microstrip lines connected to the MMIC attenuator die can be de-embedded using thru, line, reflect (TRL) calibration method [17]. The reference planes are denoted in Fig. 3. For a two-port network, TRL calibration removes the errors from the wires and connectors by measuring the S-parameters of three additional transmission line structures: Thru, a transmission line with a length equal to the length of the traces from the DUT to the edge of the board; Reflect, an open- or short-circuit on both the connectors; and Line, a transmission line with length equal to Thru plus an electrical length of about 20°–



(a) (b)

Fig. 8. Measurement setup for monotonic bending tests of inkjet-printed "ramp" interconnects. (a) Three-dimensional-printed mandrel (radius = 50, 40, 30, 20, 10, 5 mm; left to right). (b) Bent sample measured with an Anritsu 37369A VNA.

160°. At a given frequency, the goal of the calibration is to find the real ABCD matrix of the DUT $[A'B'C'D']$

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} A^m & B^m \\ C^m & D^m \end{bmatrix} \begin{bmatrix} D & B \\ C & A \end{bmatrix}^{-1} \quad (1)$$

where $[A^m B^m C^m D^m]$ is the measured ABCD matrix, and $[ABCD]$ is the ABCD matrix of the "error box" containing the wires and connectors, which is assumed to be symmetrical and reciprocal across both sides of the DUT. The following formulas from [20] are used to find $[ABCD]$. The scattering matrices for the TRL structures are given as $[T]$, $[L]$, and $[R]$, respectively. The elements of the reciprocal scattering matrix for the error box can be calculated as

$$S_{22} = \frac{T_{11} - L_{11}}{T_{12} - L_{12}e^{-\gamma l}} \quad (2)$$

$$S_{11} = T_{11} - S_{22}T_{12} \quad (3)$$

$$S_{12} = \sqrt{T_{12}\left(1 - S_{22}^2\right)} \quad (4)$$

$$e^{\gamma l} = \frac{A \pm \sqrt{[A]^2 - 4L_{12}^2 T_{12}^2}}{2L_{12}T_{12}} \quad (5)$$

$$A = L_{12}^2 + T_{12}^2 - (T_{11} - L_{11})^2. \quad (6)$$

These S-parameters are then used to construct the equivalent $[ABCD]$ matrix using the transformations in [20]. The same transformations are used to calculate the final scattering matrix for the DUT after $[A'B'C'D']$ is found using (1) and to calculate $[A^m B^m C^m D^m]$ from the measured S-parameters of the entire cascade. This process is repeated for all the frequency points along the frequency sweep to generate the final S-parameter plots versus frequency for the DUT. For each bending configuration, the TRL standards go through the same bending cycles as the prototypes before de-embedding to ensure small variations caused by the bent feedlines can be eliminated.

Figs. 5 and 6 show the de-embedded S-parameter results of the three samples, which only consider the insertion loss from the die and ramp interconnects. The average de-embedded results are plotted in Fig. 7, where the loss per ramp interconnect is calculated as the difference in the measured S_{21} value between bare die and die with two ramp interconnects, with one interconnect on each side. Compared with the bare die performance, it can be seen that each inkjet-printed ramp interconnect contributes less than 1.2-dB insertion loss over

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TABLE II
PERFORMANCE COMPARISON OF STATE-OF-ART ADDITIVELY MANUFACTURED INTERCONNECTS

	Fabrication Technology	Substrate	Interconnect Type	Frequency	Insertion Loss per Interconnect
[10]	Inkjet Printing	MEG6	CPW	24.5GHz	0.5dB
[7]	Inkjet Printing	Glass	CPW	40GHz	0.96dB
[8]	Inkjet Printing	MEG6	Microstrip line	10-40GHz	0.5dB average
[13]	Aerosol Jet Printing	LCP	Microstrip line	40GHz	0.2dB
[14]	Aerosol Jet Printing	Kapton	CPW	30GHz	0.27dB
[15]	Aerosol Jet Printing	RO4003C	Microstrip line	20GHz	1.3dB
This work	**Inkjet Printing**	**RO3003**	**Microstrip line**	**20-40GHz**	**0.27-1.16dB**

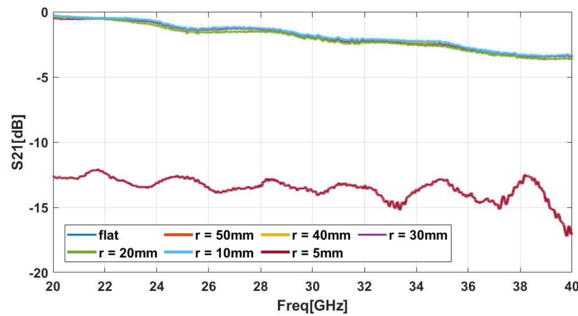


Fig. 9. S_{21} measurement results of the monotonic mandrel bending tests over different sizes of mandrels.

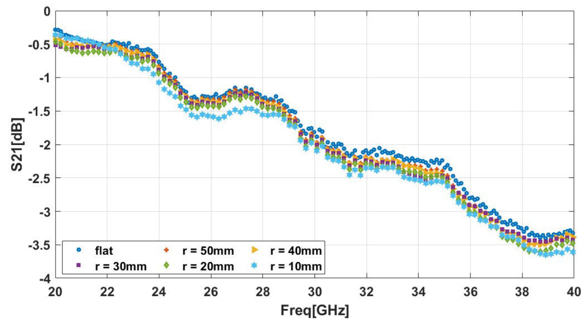
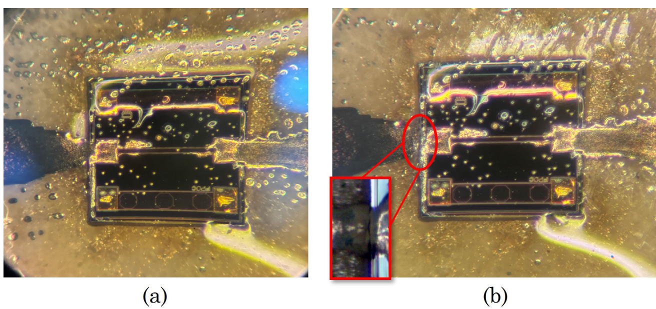


Fig. 10. S_{21} measurement results of the monotonic mandrel bending tests over different sizes of mandrels before failure.



(a) (b)

Fig. 11. Comparison of the fabricated ramp interconnects' structure (a) before and (b) after monotonic bending tests.

the whole 20-40-GHz frequency band. Table II summarizes the performance of the state-of-art additively manufactured interconnects. The insertion loss of the interconnects is determined by several factors: ink conductivity, ink metallization thickness, and interconnect structures. The proposed design in this work demonstrates similar performance with other inkjet-printed designs because the same SNP ink and the same measurement setup were used. Compared with inkjet printing, aerosol jet printing has demonstrated advanced designs at higher frequencies owing to its superior resolution, but it comes with higher operating cost due to additional necessary units to create droplet mist and focused carrier gas stream [4]. Oakley et al. [13] reported very low loss aerosol jet-printed interconnects up to 40 GHz with only 0.2-dB insertion loss per interconnect. However, their prototypes experienced cracks easily, even under flat conditions. Therefore, as highlighted earlier, the flexibility and reliability of such additively manufactured interconnects remain unexplored in previous research, which will be the main focus of Section III in this article. It is also worth noting that in this work, the bare die measurement results were conducted under different conditions by the manufacturer; therefore, the insertion loss per ramp interconnect may also include additional loss from the in-house fabrication and assembly processes, such as different die attach methods and less conductive silver epoxy. Further improvements can be realized through the utilization of highly conductive inks or adjustments to the slope and length of the ramp interconnects. Better impedance matching can also be achieved by fine-tuning and optimizing the ramp topology and dimension through 3-D full-wave electromagnetic simulations, given the accurate model of the die.

III. RELIABILITY TESTING OF RAMP INTERCONNECTS

A. Monotonic Bending Tests

To examine the durability of the inkjet-printed ramp interconnects, a series of monotonic bending tests were first conducted. Using 3-D-printed PLA mandrels ranging in size from 5 to 50 mm in outer radius, the prepared samples of die with ramp interconnects connected to microstrip lines were consecutively bent around them, facing outward. Fig. 8 shows the 3-D-printed mandrels and measurement setup. The mandrels were designed to be half-cylindrical in shape to support stable measurements. An Anritsu 37369A VNA was used to measure the S-parameter response of the sample at pre- and postbending conditions. S_{21} measurements of the sample under different radii were recorded, as depicted in Figs. 9 and 10. It can be seen that during bending over the smallest mandrel radius of 5 mm, high insertion loss was introduced from the ramp interconnects, suggesting very poor transmission. The dc resistance was also monitored during the bending test. It was noted that the measured resistance over the die with two interconnects varied between 1.1 and 1.3 Ω

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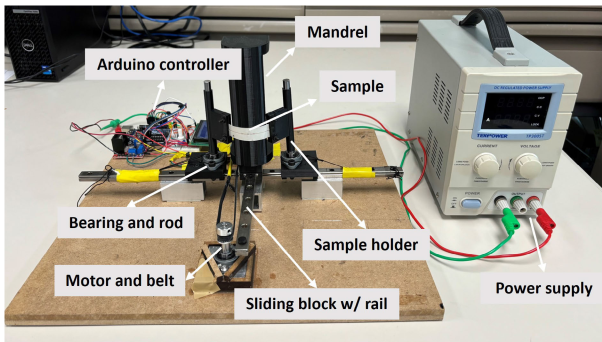


Fig. 12. Experimental setup for automated cyclic bending tests.

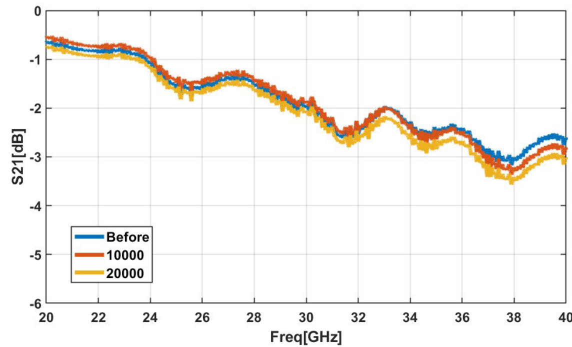


Fig. 13. S_{21} measurement results of the cyclic bending tests (mandrel radius = 10 mm).

as the bending radius decreased from 50 to 10 mm, and no resistance could be measured (open circuit) under the bending radius of 5 mm. By carefully examining the sample, cracks were observed on the printed silver trace of the interconnection lines, between the edge of the die and the SU8 dielectric ramp, as shown in Fig. 11. This is mainly caused by the very high tensile strain induced by an extreme bending radius of 5 mm, and the connection between the die and the ramps is the most vulnerable part that has the least ink coverage. Nevertheless, across mandrel sizes spanning from 50 to 10 mm in radius, the inkjet-printed ramp interconnects consistently maintained robust signal transmission, exhibiting minimal variation with less than 0.15-dB insertion loss per interconnect across the 20–40-GHz frequency band. This remarkable stability underscores their promising suitability for applications necessitating rigorous bending conditions.

B. Cyclic Bending Tests

Subsequent to the monotonic bending tests, an automated mandrel testing apparatus was developed to conduct cyclic bending assessments [11], as shown in Fig. 12. The bending radius was chosen to be 10 mm, which is the smallest radius the interconnects can sustain without deterioration in performance, based on the measurement results in Section III-A. In the experimentation setup, the fabricated sample is affixed onto the sample holder, which, in turn, interfaces with a rod-bearing mechanism permitting unimpeded rotation. This sample holder interfaces with a rack-and-rail system, affording an additional longitudinal degree of freedom to the sample holder. Thus, the movement of the mandrel toward the sample

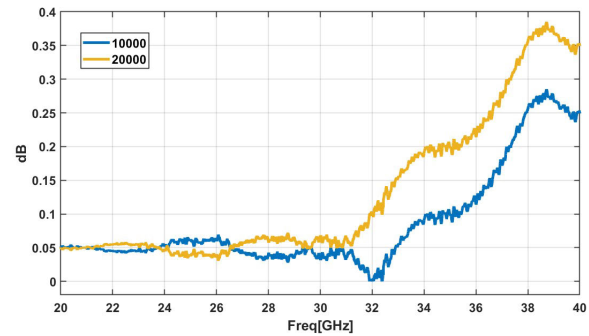
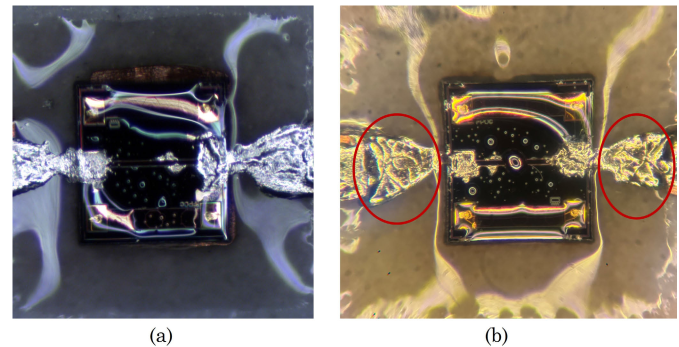


Fig. 14. Measured difference in insertion loss of the inkjet-printed "ramp" interconnects during cyclic bending tests compared with initial state without bending.



(a) (b)

Fig. 15. Comparison of the fabricated ramp interconnects' structure (a) before and (b) after cyclic bending tests.

TABLE III
MEASUREMENT OF DC RESISTANCE DURING CYCLIC BENDING TEST

Bending cycles	**Before**	**After 10000**		**After 20000**	
		bent	**flat**	**bent**	**flat**
DC resistance (Ω)	1.4	1.6	1.2	1.8	1.5

reconfigures it from its initial state to a bent state, ensuring the sample conforms entirely to the mandrel with minimal stretching. An elastic cable affixed horizontally to the sample holder's end ensures the sample can return to a flat state once the mandrel moves away. The Arduino-controlled translation of the mandrel is executed through a motor-belt system connected to a sliding block on a rail. S_{21} measurements are obtained initially with the sample placed flat before any bending tests and subsequently after the prescribed number of cyclic bending cycles.

The experimentation encompassed pre- and postbending S_{21} measurements following 0, 10 000, and 20 000 bending cycles across the sample. As illustrated in Fig. 13, the fabricated ramp interconnects maintained consistent S_{21} readings throughout the bending cycles up to 20 000 times. In addition, the outcomes reveal a slight increase in insertion loss corresponding to the bending cycles, apart from the deviations between each measurement. The variations in insertion loss of the sample after bending compared with before bending are plotted in Fig. 14. It can be noted that at 36–40 GHz, cyclic bending introduced 0.2–0.4 dB more loss, while at 20–30 GHz, there is not much difference between before and after bending

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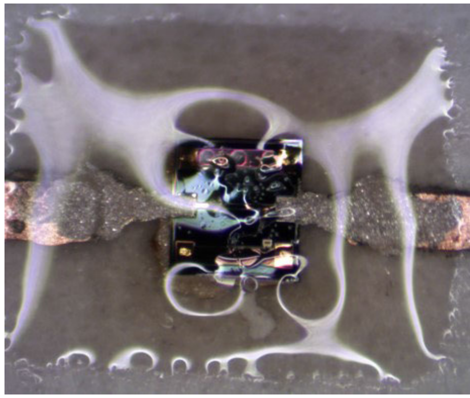


Fig. 16. Inkjet-printed ramp interconnects’ prototype interfacing an MMIC GaAs attenuator die with SU8 encapsulation.

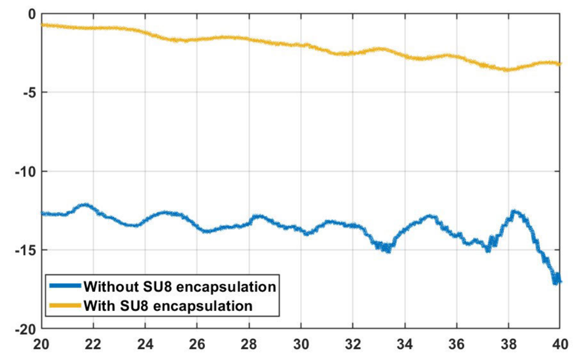
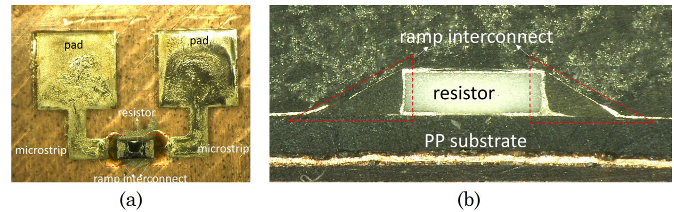


Fig. 17. Measured S_{21} of fabricated samples with and without SU8 encapsulation at bending radius = 5 mm.



(a) (b)

Fig. 18. Demonstration of inkjet-printed ramp interconnects interfacing a zero-ohm thin-film resistor [11]. (a) Fabricated prototype of inkjet-printed ramp interconnects for the resistor. (b) Crosssectional examination of the interconnects.

conditions. This can be attributed to fatigue-related failures within the printed ink structure, as depicted in Fig. 15, where small cracks were generated on the surface of the inkjet-printed silver interconnects during cyclic bending. Due to the fact that RF performance is more sensitive to surface imperfections of the conductors at higher frequencies, a more obvious change can be observed at 36–40 GHz. The detailed evaluation of RF performance related to ink failure at different metallization thicknesses can be found in the previous research [11]. In addition, the measured dc resistance of the fabricated prototype demonstrates a minimal variation from 1.4 to 1.8 Ω during cyclic bending, as shown in Table III. The resistance under bent conditions is higher than that under flat conditions because the cracks become more prominent during bending. Overall, after 20 000 times of cyclic bending tests, the fabricated ramp interconnects were able to maintain good transmission performance, demonstrating 1.36-dB insertion loss per interconnect at 40 GHz with 0.2-dB increment compared with before bending, striking a balance between robust electrical characteristics and mechanical reliability for applications in flexible and wearable 5G mmWave contexts.

IV. Discussion

One of the unique advantages of using additive manufacturing is the ability to deposit various materials in a highly customized fashion. Oakley et al. [13] demonstrated the rework of the printed silver trace by depositing thicker silver layers to cover the cracks on the interconnects generated during measurements. The measured S_{21} has shown great improvements compared with the case before repair. To extend based on this idea, this article proposed to create encapsulation using SU8 dielectric ink for the ramp interconnects, where two layers of SU8 in a square shape are deposited on top of the fabricated sample to cover the MMIC die, the ramp interconnects, and part of the microstrip lines, as show in Fig. 16. This encapsulation can both protect the fragile parts of the ramp interconnects and enhance the mechanical strength of the attachment. The measured S_{21} results for the encapsulated sample are shown in Fig. 17. By adding the additional protection, the sample can withstand a smaller bending radius of 5 mm, with less than 0.1-dB added insertion loss, showing the potential for applications under extreme flexing conditions.

In addition, leveraging the tailored “staircase” printing method proposed in this work, the envisaged ramp interconnects exhibit versatility in application across diverse components of varying dimensions. A surface-mount zero-ohm thin-film resistor was used as an example [11], as illustrated in Fig. 18. The resistor, measuring 900 μm in length, 450 μm in width, and 300 μm in height, was positioned at the center of a 60-mm-long and 15-mm-wide 3-D-printed flexible polypropylene (PP) substrate featuring a copper tape acting as the ground plane. The ramp interconnects were printed on both sides of the resistor with 600 μm in length, featuring a slope angle around 26°, to establish connections to a short 1.5-mm-long microstrip line linked to a resistance measurement pad. Using the same bending test configuration from Fig. 12, evaluations were conducted using a mandrel with a 1-in radius to assess the bending reliability of the ramp interconnect. Prior to any bending and after 10 000 bending cycles, resistance measurements were taken at the two pads. A consistent resistance level was maintained throughout the entire 10 000 cycles, indicating the sustained functionality of the interconnects with different dimensions.

However, elevating the slope angle of the ramps introduces a potential for increased failure during bending. From a mechanical standpoint, the constructed ramp interconnects’ structure manifests stress concentration on the printed ink situated at the base of the ramp. Consequently, at steeper slope angles, the interconnects exhibit a less smooth geometric transition, encountering elevated stress levels during bending. In addition, ink accumulation intensifies at the bottom edge of the ramps, resulting in nonuniform curing and more initial defects, thereby raising the likelihood of failure. Nevertheless, the SU8 encapsulation method, as mentioned earlier, holds promise in

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mitigating this potential challenge by offering added protection to both the MMIC and the ramp interconnects. In addition, considering the existing large CTE mismatch between SU8 and semiconductor material, preliminary thermal tolerance testing was performed. The printed module was able to maintain its performance after going through a thermal cycle ramping from 25 °C to 160 °C within 1 h in the oven. Future research efforts can delve into assessing inkjet-printed ramp interconnects with varied slope angles or dimensions over diverse bending radii, as well as mechanical reliability under comprehensive thermal cycling tests.

V. Conclusion

In this article, the inkjet-printed 3-D ramp interconnects have been designed, fabricated, and evaluated for their electrical and mechanical reliability under various bending conditions over 20–40 GHz, showcasing the applicability for both active MMICs and passive components over a wide spectrum of 5G mmWave frequency bands. The proposed unique fabrication process, differentiated from all previously reported methods, enables superior rugged ramp interconnects for curved surfaces and can be easily adapted to components of different sizes on both rigid and flexible substrates. The RF characterization of the fabricated samples with ramp interconnects interfacing with an MMIC attenuator die highlights a minimal insertion loss of 0.18–1.16 dB per interconnect from 20 to 40 GHz. Through the monotonic bending and cyclic bending tests, the fabricated prototypes proved to maintain excellent RF performance with less than 0.2-dB variation in insertion loss per interconnect up to 40 GHz during 20 000 times of cyclic bending over the mandrel with 10 mm in radius, demonstrating good reliability from both electrical and mechanical perspectives. In addition, with inkjet-printed SU8 dielectric encapsulation, the fabricated sample can withstand a smaller bending radius of 5 mm, suggesting potential applications under extreme flexing conditions. By leveraging low-cost and scalable additive manufacturing technologies, the proposed interconnects could facilitate rapid prototyping and deployment of flexible wireless packages across diverse environments. The results reported in this article lay a foundation for future endeavors focused on creating highly customizable, heterogeneously integrated, high-performance flexible SoP and MCM for 5G mmWave wearable and conformal applications.

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