Ultrathin Antenna-Integrated Glass-Based Millimeter-Wave Package With Through-Glass Vias

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***Abstract*— This article presents the design and demonstration of a high-bandwidth antenna-in-package (AiP) module focusing on low-loss interconnects and Yagi–Uda antenna performance fabricated on a 100-μm low coefficient-of-thermal-expansion (CTE) glass for the 28-GHz band. It shows the modeling, design, and characterization of key technology building blocks along with the process development of advanced 3-D glass packages. The building blocks include impedance-matched antenna-to-die signal transitions, Yagi–Uda antenna, and 3-D active–passive integration with backside die assembly on 100-μm glass substrates. The design and stack-up optimization of antenna-integrated millimeter-wave (mm-wave) modules is discussed. Process development to achieve high-density interconnects and precise dimensional control in multilayered thin glass-based packages is also described. The characterization results of the key technology building blocks show an insertion loss of 0.021 dB per through-package via (TPV), leading to the whole-chain loss of less than 1 dB and a return loss lower than 20 dB. The fabricated Yagi–Uda antenna features high repeatability of wide bandwidth due to the process control enabled by glass substrates. The antenna measurements show a bandwidth of 28.2%, which covers the entire 28-GHz fifth-generation (5G) frequency bands (n257, n258, and n261). The flip-chip assembled low-noise amplifier with 80-μm solder balls shows a maximum gain of 20 dB as desired. The performance of the glass-based package integrated antennas is benchmarked to other 5G substrate technologies, such as organic laminates or co-fired ceramic-based substrates.**

***Index Terms*— Antenna-in-package (AiP), fifth-generation (5G), glass substrate, millimeter wave (mm-wave), packaging.**

I. Introduction

HETEROGENEOUS and 3-D integration of active and passive components has become the key strategy to realize high-performance millimeter-wave (mm-wave) systems for emerging fifth-generation (5G) mobile communications. Innovative packaging architectures such as antenna-integrated modules are sought for all classes of 5G-enabling products, such as handsets, customer premises equipment, and base stations. From the system integration point of view, low interconnect signal losses from chip to antenna coupled with high-gain high-bandwidth antennas are required to achieve superior system performance [1], [2]. Advanced packaging substrates and low-loss thin-film build-up dielectrics, codesign of actives, passives, antennas, and their 3-D integration in mm-wave bands, are therefore widely pursued by the industry [3]–[5] and academia [6]–[8].

State-of-the-art packaging technologies in mm-wave modules include low-temperature co-fired ceramic (LTCC) substrates [9], [10], low-cost printed-circuit board (PCB) processes, advanced organic substrates [4], [11], and fan-out wafer-level packages (FOWLP) with epoxy molding compounds [12], [13]. LTCC substrates have advantages, such as low-loss properties at high frequencies and low moisture absorption [14]. The limitation of the cost and the difficulty in large-panel scalability of ceramic substrates, however, led to the prevalence of organic substrates [15]. Although LTCC substrates provide higher reliability, lower shrinkage, and smaller feature sizes [16] than multilayered organic substrates, the minimum line-and-space remains 40 μm due to the thick-film co-firing processes. In conventional processes, copper-clad laminates and prepreg are compressed to form low-cost multilayered organic substrates [5], [17], [18]. The main challenge is the limitation of small features (>80 μm) caused by layer-to-layer alignment inaccuracy and substantive etching processes. The relatively coarse patterning leads to an increase in the metal-layer counts. The through-hole vias are generally more than 200 μm, which hinders miniaturization and high-density packaging. In addition, these substrates cause warpage throughout the fabrication processes, which results in degraded electrical performance and reliability issues after the assembly of active and passive components. The most recent approach utilizes build-up layers on a rigid core substrate [7], [11]. High-density interconnects in build-up layers can potentially enable complex signal routing and

Manuscript received April 1, 2020; revised June 10, 2020 and July 16, 2020; accepted August 4, 2020. Date of publication September 21, 2020; date of current version December 3, 2020. *(Corresponding author: Atom O. Watanabe.)*

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Digital Object Identifier 10.1109/TMTT.2020.3022357

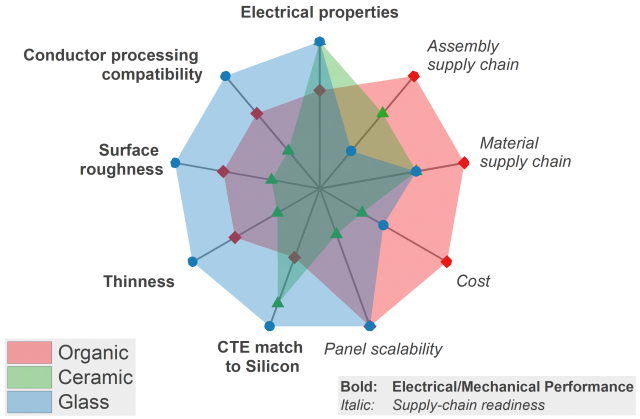

Fig. 1. Comparison of three primary substrate materials used for 5G mm-wave applications.

reduce the metal-layer counts [19], leading to the thickness reduction of the entire modules. The elements accommodated in the package are interconnected with transmission lines, through-package vias (TPVs), and microvias.

Fig. 1 shows the advantages and disadvantages of each substrate technology. Organic substrates lead to several fundamental challenges in achieving high precision and tolerance below a few micrometers. These attributes are important for precise control of impedance of high-frequency circuit elements [20]. Deviation from the desired dimensions induces frequency shifts and malfunction of such modules. Glass-based packaging has been drawing attention as an alternative solution to address these challenges in antenna-in-package (AiP) [21], [22] and integrated passive devices (IPDs) [23], [24] because of its ability to form fine-pitch line and spaces and through-glass vias (TGVs) [19], [25], [26], dimensional stability, surface smoothness ($<$10 nm), robustness against high temperature and humidity, matched coefficient of thermal expansion (CTE) with silicon dies, and large-area low-cost panel-scale processability [27]–[29]. It also features tailorability of dielectric constants (Dk) of 3.78–8 ppm/K and loss tangents ($>$0.0003) [30]–[32]. CTE can be tailored between 3 and 8 ppm/K depending on the materials used for integrated circuits (ICs) and PCBs. These parameters provide electrical and mechanical engineers with more design flexibility [33]. However, one of the evident challenges is the lack of supply chain readiness.

This article presents the design and demonstration of a high-bandwidth AiP module focusing on low-loss interconnects from chip to antenna with a 100-μm low-CTE glass, in the 5G mm-wave frequency bands (i.e., n257, n258, and n261). Section II introduces the stack-up of the package and key design rules to miniaturize the antenna-integrated package with low-loss interconnects that are matched to the designed system impedance. While the development of redistribution layers (RDLs) on glass is discussed in [7], Section III focuses on the via-in-via vertical interconnects and fine-pitch IC assembly that are critical to obtain the desired electrical performance of package-integrated antennas and active ICs. In addition to the fundamental characterization of transmission lines performed in [19], this article shows,

TABLE I
STACK-UP OF THE FOUR METAL-LAYERED GLASS-BASED ANTENNA MODULE

M1	Antenna patterns, feedlines, transmission lines
	15-μm build-up polymer
M2	Partial ground plane
	15-μm build-up polymer
	100-μm glass core
	15-μm build-up polymer
M3	Partial ground plane
	15-μm build-up polymer
M4	Transmission lines, bump pads, power plane

in Section IV, the detailed characterization of low-loss chip-to-antenna interconnects with transmission lines and TPVs in the wider frequency band, high-bandwidth Yagi–Uda antennas, and IC assembly on the fabricated glass substrates. In conjunction with the comparison of the proposed work with recent leading-edge reports (see Section V), the conclusions are compiled in Section VI.

II. DESIGN OF THE STACK-UP OF THE ANTENNA-INTEGRATED GLASS-BASED MM-WAVE PACKAGE

This section discusses the design of the four metal-layered mm-wave modules, including the antenna patterning, die assembly, signal routing, and power distribution. The stack-up is shown in Table I. The module design begins with antenna selection and placement. A well-known dipole Yagi–Uda antenna with one director and a balun is designed and implemented on the top metal layer (M1) in the test vehicle to meet the bandwidth that covers 24.25–29.5 GHz. Yagi–Uda antennas feature a main lobe in the azimuth plane with a single polarization, while the most radiation of patch antennas directs in the vertical plane. The selection of antennas depends on the application of the modules to be implemented. The main advantages of the dipole Yagi–Uda antenna are the design simplicity, wide bandwidth, and control of the gain of the main lobe by changing the number of directors.

In this test vehicle, the dipole Yagi–Uda antenna is fed by a microstrip line transitioned from a ground-backed coplanar waveguide (GCPW). Coplanar waveguide (CPW) or GCPW signal routing is more common for multilayered package than microstrip lines or striplines because of their inherent shielding features and minimal crosstalk with other nearby transmission lines or components. Electromagnetic waves are tightly confined between the signal paths and the adjacent ground planes, which prevents antenna radiation from being interrupted and degraded. The GCPW approach also enables designers to control and achieve a wide variety of impedance simply by adjusting the spacing between the grounds and the signal line without changing the thickness of the dielectric. The partial ground plane in M2 is incorporated for the GCPW signal distribution. In mm-wave frequencies (20 GHz and above), dielectric loss in multilayered signal routing dominates the package loss budget, resulting in high demand for low-loss-tangent (tan δ) dielectric materials to maintain the signal integrity and mitigate signal losses in the package.

The partial ground plane placed in M2 is interconnected with the ground plane in M3, which serves as a ground plane for the Yagi–Uda antenna and GCPW signal traces in the M4 layer. The GCPW formed in M4 interconnects with TPVs as a feed line of the Yagi–Uda antenna. The signal TPVs are surrounded by two grounded TPVs, where the impedance of TPVs is controlled by changing the pitch between the signal and ground TPVs. The impedance control in TPVs is critical to achieve impedance matching and high bandwidths of package-integrated antennas. Specifically, the GCPW alone [see Fig. 5(a)] is designed to be slightly capacitive and less resistive than the target impedance since TPVs usually add more resistance and inductive reactance [see Fig. 5(b)]. The characteristic impedance of the GCPW is therefore designed to be $(46 - j0.44)\ \Omega$. The designed GCPW consists of a signal width of 27 μm and a space of 44 μm with a 15-μm build-up dielectric (ABF GL102: Dk = 3.3 and Df = 0.0044 at 5.8 GHz).

The landing pads on the package-side interconnecting dies and discrete passive components (e.g., bypass capacitors) are designed to have a diameter of 120 μm, whereas the solder ball size is approximately 80 μm and the pitch is 200 μm. The dies and passives are flip-chipped underneath the M4 layer to hinder those assembled components from interfering with the Yagi–Uda antenna and to effectively miniaturize the package, as shown in Fig. 4. Direct current (dc) voltage with a bias of 5 V is supplied from the M4 layer, while bypass capacitors of 0.1 μF and 100 pF are mounted no farther than 0.7 mm from the low-noise amplifier (LNA) to short alternating-current (ac) signals to ground producing clean and pure dc signal.

III. Process Development

This section discusses the development of the process and chip assembly methodology that forms circuitry and provides high-density low-loss interconnects and high precision of RDLs on a package core substrate.

Thin alkali-free boro-aluminosilicate glass core substrates with vias predrilled by AGC Inc. (formerly Asahi Glass Company, Ltd.) are employed for the test vehicles. The TGVs were designed to have a diameter of 80 μm. The 6-in square panels with 100-μm thickness are used for the process demonstration. This technology is compatible with large-area panel-level packaging, which is widely being commercialized recently [34], [35]. It potentially allows obtaining 4.54 times more coupons on a panel with 500 mm $\times$ 500 mm, which also lowers the cost compared with a traditional 12-in round wafer used for fan-out wafer-level packaging. Appropriate handling procedures are critical for glass substrate fabrication processes in order to address the brittleness and fragility of ultrathin glass. The lamination of thin dielectric films is the key to compensate for the brittleness of thin glass substrates. The dielectric properties are listed in Table II. Notably, the adhesion of dielectric materials for build-up layers to copper metal patterns and glass substrates is improved compared with the test vehicles in [7] and [19]. The fabrication process of the high-density interconnects formed in RDLs is summarized in Fig. 2 and discussed in [7] and [36] with more details.

TABLE II

Material Properties Utilized in the 3-D Glass-Based Antenna Module

Materials	Glass core	Build-up dielectric
Dk	5.4	3.3
Df	0.006 @ 28 GHz	0.0044 @ 10 GHz
CTE (ppm/K)	3.8	49
Thickness (μm)	100	15

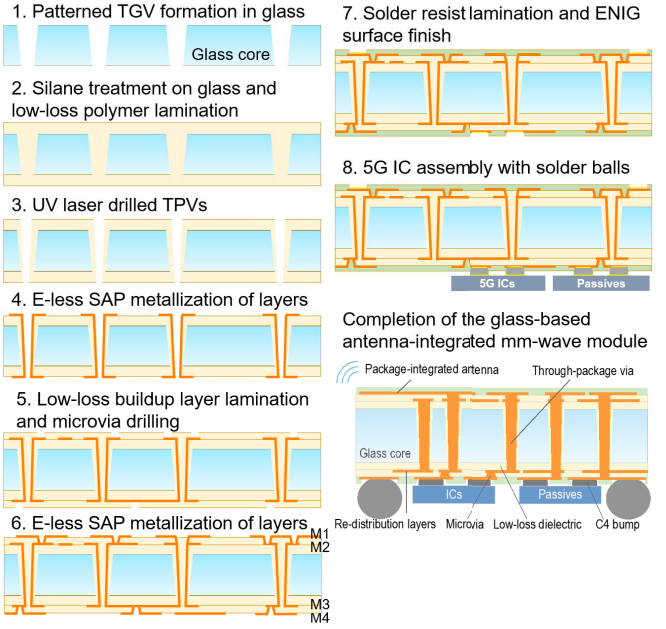

Fig. 2. Fabrication process of highly integrated mm-wave packages with the via-in-via process, RDL formation, and the assembly of ICs and passive components.

Upon the completion of multilayer fabrication on a glass core laminated with thin-film dielectric, solder-resist films provided by Taiyo Ink. are laminated on both sides of the package substrate to prevent the outermost surface from being oxidized or damaged. This process is also shown in Fig. 2. We designed solder-mask-defined (SMD) chip-to-package interconnects, which effectively reduces the size of the copper pad that the component is soldered to. To prevent oxidation of copper traces and pads and suppress intermetallics formation, a thin layer of electroless-nickel immersion gold (ENIG) is deposited, followed by the placement solder balls with a diameter of 80 μm approximately on 80-μm pads with a pitch of 200 μm. The gallium-arsenide (GaAs)-based dies are assembled with a flip-chip mounter, whereas several passive components, such as bypass capacitors, are surface-mounted with solder paste. The solder balls and solder paste are reflowed altogether at the end of the fabrication. The cross-sectional images with TPVs and dies assembled are shown in Fig. 3, while the top-view inspection is performed through an X-ray microscope and the image is shown in Fig. 4.

IV. Characterization of Key Building Blocks

To characterize the fabricated four-metal-layer test vehicles on glass substrates, high-frequency measurements of transmission lines, and TPVs as interconnects, package-integrated

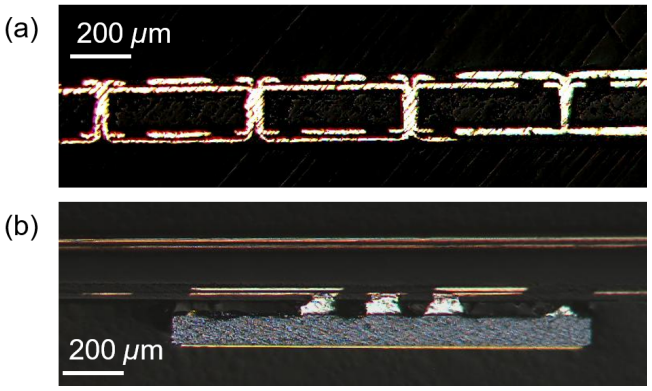

Fig. 3. Microscope cross-sectional images of fabricated panel with the four RDLs. (a) TPVs, microvias. (b) Assembled LNA using 80-μm solder balls.

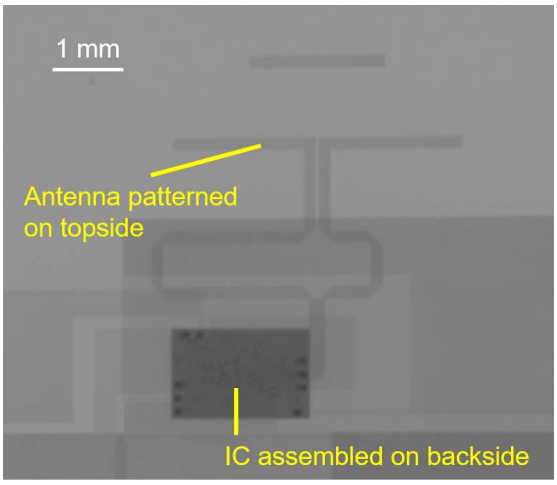

Fig. 4. X-ray inspection of the test vehicle that integrates a Yagi–Uda antenna, impedance-matched interconnects, TPVs, and an assembled LNA.

Yagi-Uda antenna, and a flip-chip-assembled LNA are performed through a vector network analyzer (VNA) that is calibrated up to 40 GHz.

A. Characterization of Low-Loss Interconnects

While the copper thickness is 8 μm in all the layers of this package, the width and space of the designed GCPW were 27 and 44 μm, respectively. However, the photomask for lithography was designed differently, considering overetching of metal patterns. As the semiadditive patterning (SAP) process overetch approximately 0.5–1 μm, the width and space were 29 and 42 μm on the photomask, respectively. As designed from the electrical and process standpoints, the fabricated GCPW showed the precise linewidth and space, which are 27.3 and 43.3 μm, respectively, as shown in Fig. 5(a). Based on the fabricated interconnect structures (see Fig. 6), S-parameters were measured to quantify the signal losses induced by the interconnects between the antenna and IC. The interconnects include 2-mm GCPW and two TPVs (see Fig. 5). The S-parameters for the structures with and without TPVs are plotted in Fig. 7. As discussed in Section II, GCPWs are formed in M1 and M4 with TPVs interconnected.

While the article [19] shows the insertion loss of transmission lines on a 100-μm glass substrate in the

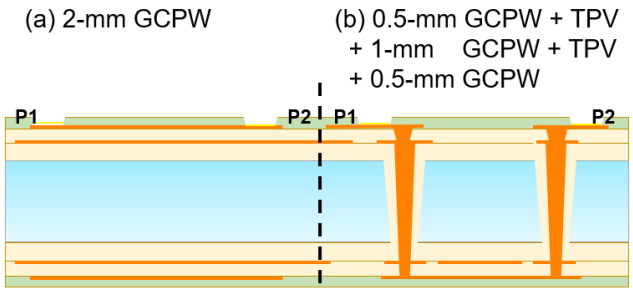

Fig. 5. Design and stack-up of several interconnects used in this test vehicle. (a) Transmission line. (b) Transmission lines with TPVs.

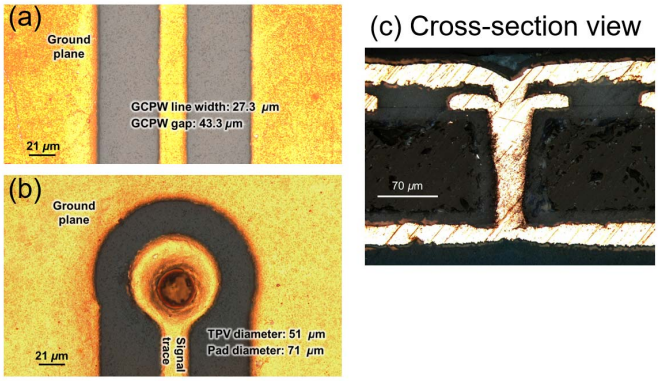

Fig. 6. Package-level interconnects. (a) Top view of GCPW. (b) Transition from GCPW to TPV. (c) Cross-sectional view of TPV connecting M1, M2, and M3 altogether.

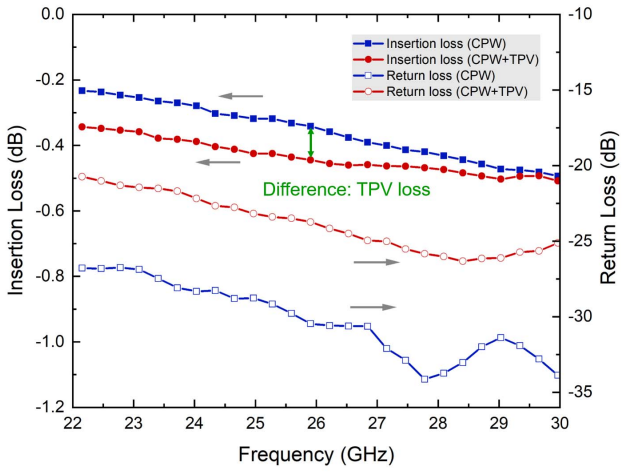

Fig. 7. Measured S-parameters of the glass-package interconnects with and without TPVs.

narrowbands (26–30 GHz) and poor impedance matching with rippled frequency responses, the characterization results in this article present the impedance-matched GCPWs and TPVs to the 50-Ω system, leading to low voltage standing-wave ratio (VSWR) in the target frequency range (24.25–29.5 GHz). In addition to the pad-to-via impedance continuity, the impedance of TPVs is adjusted by manipulating the diameter (50 μm) and the pitch (200 μm). In addition to the low insertion loss, the results (see Fig. 7) indicate the return losses of higher than 20 dB in the whole frequency band of interest (22–30 GHz). The Smith chart (see Fig. 8) also

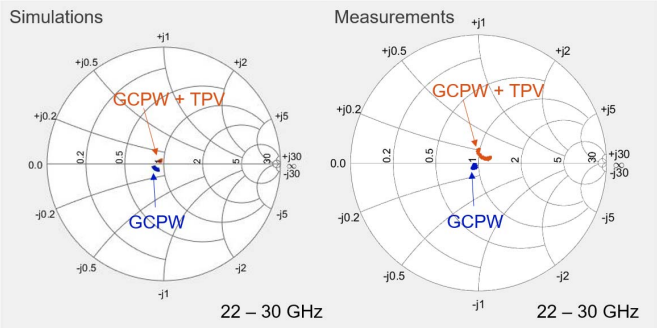

Fig. 8. Smith chart showing return losses from GCPW and the chain of GCPW with two TPVs in the frequency range from 22 to 30 GHz.

shows the well-matched input impedance for both the GCPW line and the chain of GCPW and TPVs. While the real parts of their input impedance are close to 50 Ω, the reactance of the structure with TPVs is 7.04 Ω higher in measurements, which is attributed to the inductive parasitics from TPVs [37]. However, the design with consideration of the inductive effect assisted the impedance of the chain with TPVs to match 50 Ω, resulting in the low return loss higher than 20 dB in the entire frequency range of interest.

The measured insertion loss of GCPW with solder resist without TPVs was 0.216 dB/mm at 28 GHz. The simulated insertion loss of GCPW alone is 0.119 dB/mm without the solder resist. The addition of solder resist leads to the simulated insertion loss of 0.178 dB/mm at 28 GHz. This 50% increase is mainly attributed to the loss tangent of solder resist (Df = 0.02 at 1 GHz). Thus, it is critical to design circuitry in outermost layers considering the properties of a solder mask. The evident signal loss due to solder resist leads to a demand for low-loss solder resist for mm-wave applications.

Based on the measured GCPW insertion loss, the insertion loss caused by TPVs was measured by subtracting the insertion loss of the chain [see Fig. 5(b)] from GCPW [see Fig. 5(a)], in which the length of the GCPW is kept identical. The measured TPV loss was 0.021 dB/TPV. The controlled diameters of landing pads and antipads [see Fig. 6(b)] also affect the signal transition from the electromagnetic-wave standpoint. Compared with traditional through-hole vias in multilayered organic substrates, where comparatively large vias (>500 μm) are drilled mechanically, TGVs with the via-in-via process are beneficial in achieving small dimensions (i.e., diameters and pitches) with better control for high-density interconnects and managing signal integrity.

The via-in-via process in glass substrates connects multiple layers without the need for rerouting signal traces in-plane and vertically connecting RDLs with blind vias. The TPV in Fig. 6(c) interconnects the top metal layer (M1) to feed antennas and the second bottom layer (M3) directly. This advantage offers space reduction for signal routing, seamless impedance continuity, and design flexibility to radio frequency (RF) designers. Glass substrate technology offers highly accurate layer-to-layer alignment, which enables the pad size closer to the diameter of vias. The small via pads and spacing lead to low parasitic capacitance between via pads in multiple layers and low impedance discontinuity.

TABLE III
PARAMETERS USED FOR THE ANTENNA DESIGN

Parameters	Values	Parameters	Values
w_{ant}	180 μm	w_{bal}	180 μm
d_{dir}	1.18 mm	l_{bal}	0.82 mm
d_{gnd}	1.09 mm	w_{ant}	220 μm
s_{cps}	50 μm	l_{ant}	2.2 mm
w_{cps}	180 μm	w_{ant}	180 μm

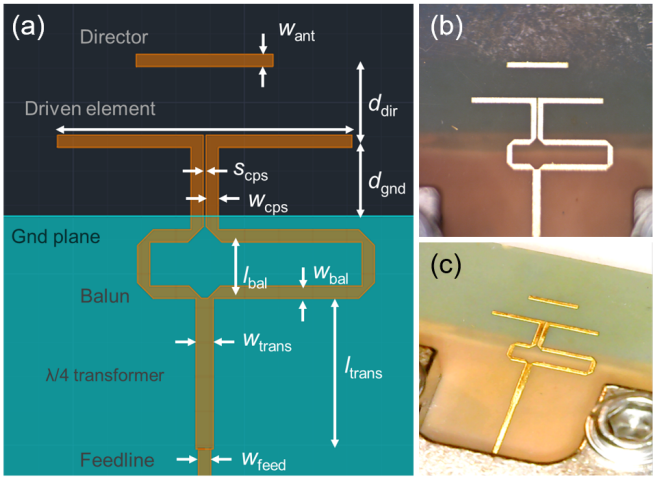

Fig. 9. Fabricated package-integrated Yagi-Uda antenna. (a) Overview with key parameters. (b) Top overview of the antenna. (b) Diced Yagi-Uda antenna element assembled with a 2.92-mm end launch connector. (c) Trimetric view.

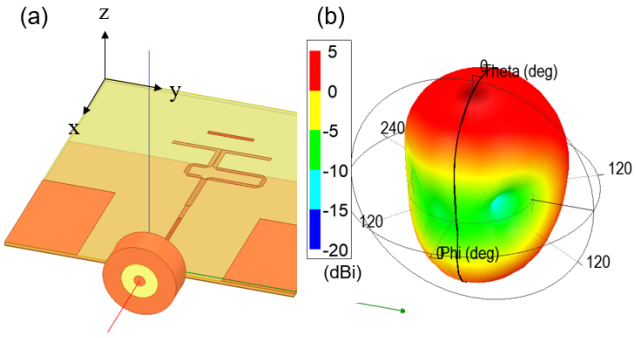

Fig. 10. Designed wideband package-integrated Yagi–Uda antenna. (a) 3-D overview of the antenna. (b) Simulated radiation pattern.

The fabricated test vehicle, as shown in Fig. 6(b), shows the margin of 10 μm on either side of TPVs.

B. Characterization of Yagi–Uda Antenna on Glass

The designed Yagi–Uda antenna is shown in Fig. 9(a) with the detailed parameters of the antenna, which are listed in Table III with values. While the fabricated antenna is shown in Fig. 9(b) and (c), the 3-D view for simulations is shown in Fig. 10(a) with the radiation pattern in Fig. 10(b). To characterize the fabricated Yagi–Uda antenna that is patterned on thin-film dielectric (M1) laminated onto the glass core, the panels were first singulated utilizing an automatic dicing machine (Disco Corporation), and a 2.92-mm end-launch connector was mounted onto the feed line connected to a Yagi–Uda antenna patterned on the top layer of the package, as shown in Fig. 9. Fig. 11 shows the in-plane (E) and out-of-plane (H) radiation patterns of the single-polarized

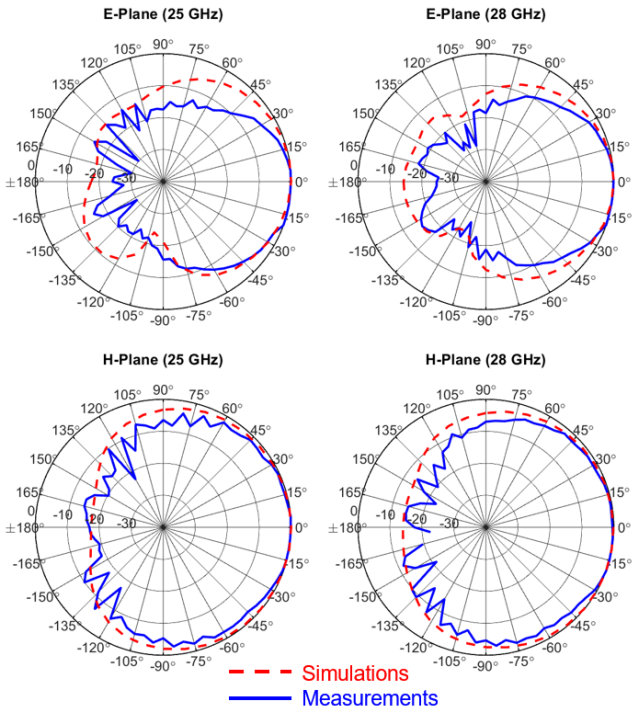

Fig. 11. Simulated (red line) and measured (blue line) in-plane (E) and (H) radiation patterns with normalized gains. The director of the Yagi–Uda antenna is placed in the direction of $\theta = 90°$ and $\phi = 0°$.

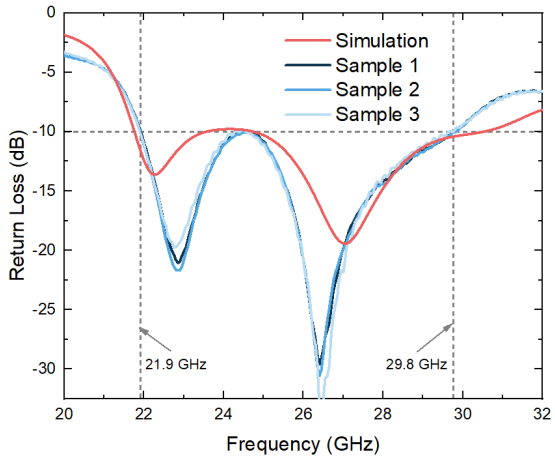

Fig. 12. Measured return loss of three antennas fabricated in the four-metal layered test vehicle to validate the consistency of frequency responses of the antennas across the glass panel.

Yagi–Uda antenna, with a comparison between the simulations and measurements. The main lobe is more directive in the E-plane because of the linear-polarization feature of the antenna, whereas the radiation patterns in the H-plane is wide-angled. The radiation patterns in the E- and H-planes show good consistency at 25 and 28 GHz. It is critical for antennas to show similar radiation patterns throughout the frequency band of interest for versatile usage of those antennas in electronic devices.

The simulated and measured return losses of patterned Yagi–Uda antennas are plotted in Fig. 12. The Yagi–Uda antenna is designed to have a double resonance to increase the bandwidth. One null at 22.3 GHz comes from the dipole,

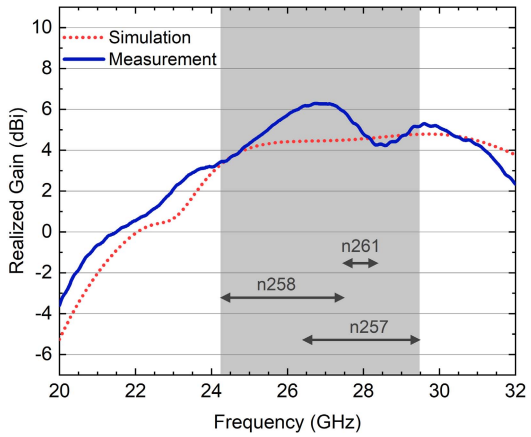

Fig. 13. Realized gain of the fabricated antenna in the direction of $\theta = 90°$ and $\phi = 180°$.

whereas the other null at 27.1 GHz results from the quarter-wave transformer. This double resonance provided the 10-dB return losses in the frequency range, 21.9–29.8 GHz, with a center frequency of 25.85 GHz. This indicates that the Yagi–Uda antennas fabricated on a 100-μm glass substrate cover the entire frequency band of interest used for 28-GHz-based 5G communications (24.25–29.5 GHz). The fractional bandwidth is 28.2% around 28 GHz, supporting the key frequency spectra (n257, n258, and n261) in the Frequency Range 2. Notably, the three Yagi–Uda antennas randomly selected from the fabricated glass panel show high repeatability of return loss. This high repeatability results from the high precision of fabrication enabled by the dimensional stability, thickness control, and surface flatness of glass substrates. The observed deviation in the smallest feature, 25 μm, was less than 2 μm with a high accuracy of the layer-to-layer alignment.

The realized gain is measured using a standardized octave horn antenna, which shows a realized gain of 20 dBi and covers a frequency range of 18–40 GHz. The measured realized gain of the fabricated package-integrate Yagi–Uda antenna is plotted in Fig. 13. The result showed a good model-to-hardware correlation and a realized gain higher than 3.44 dBi in the targeted frequency bands.

C. Characterization of Flip-Chip-Assembled LNA

In RF receiving architectures, signals from antenna arrays are delivered to LNAs to amplify the very low-power signals that are received from the antenna. Package-level interconnections assist ICs and packages to communicate with each other to external interfaces. In order to address the trend toward high-frequency networks, a higher number of input and output (I/O) are entailed to enable complex beamforming, higher data rate, and faster signal processing. Advances in IC design with system-on-chip (SoC) technology along with ultrashort die-to-package interconnections with low signal losses are required to realize the high-frequency modules. Solder ball technology is often utilized as the mainstream option for RF packages due to its cost effectiveness and the self-alignment feature during reflow assembly. Although the copper-post interconnection solutions that are mainly employed for high-performance

TABLE IV
COMPARISON BETWEEN THIS WORK AND THE PREVIOUS RELATED WORK

Work	Substrate	Frequency (GHz)	FBW (%)	Gain (dBi)	Size (λ_0)	Thickness (λ_0)	Pattern	Antenna
[38]	PCB	27.1 – 29.75	9.3	5.7	0.45 × 0.45	0.045	Azimuth	Yagi-Uda
[39]	PCB	24.5 – 31.72	25.7	4.5	0.82 × 1.98	0.056	Azimuth	SIW dipole
[40]	LTCC	26.3 – 29.79	12.4	3.1	0.18 × 0.18	0.090	Elevation	Patch
[15]	Multi-layer organic	30 – 30.8	2.6	4.9	0.6 × 0.6	0.082	Elevation	Patch
[41]	Glass	47.2 – 67	33	3.5	0.82 × 1	0.060	Azimuth	Taper-slot
This work	Glass with build-up	21.9 – 29.8	28.2	4.8	0.34 × 0.40	0.028	Azimuth	Yagi-Uda

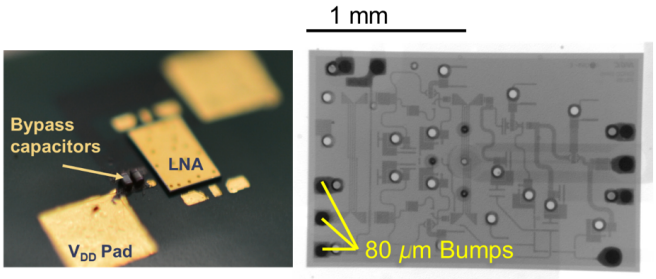

Fig. 14. 3-D view of the backside of the package (left) and X-ray inspection of solder balls mounted on SMD pads (right).

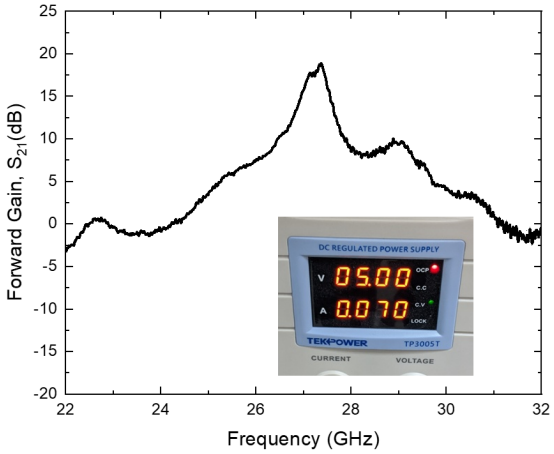

Fig. 15. Forward insertion loss, S_{21}, of the flip-chip-assembled LNA with bypass capacitors surface-mounted nearby. Inset: voltage and current supplied to the packed LNA.

computing provide low signal losses due to the higher conductivity of copper than that of solder, the approach is considered cost ineffective and impractical for RF packages. In this test vehicle, flip-chip interconnection is demonstrated with solder balls with a diameter of 80 μm, whereas the pitch of SMD pads is 200 μm, which gives enough space to prevent solder balls from shorting. In order to show short and fine-pitch interconnections using solder balls with low insertion loss, the assembly of LNA and bypass capacitors is performed with solder reflow assembly, also known as controlled collapse chip connections (C4). The assembled LNA is a product from Analog Devices [42], which covers the frequency range of 24–40 GHz.

Optical micrographs of the flip-chip assembled LNAs are shown in Fig. 14. State-of-the-art RF packages employ a pitch of 200–300 μm with a solder ball diameter of approximately 80–100 μm [4], [14]. The measured forward voltage gain, S_{21}, is plotted in Fig. 15 with intended voltage (5 V) and current (0.065–0.07 A) supplied to the packed LNA, as shown in the inset of Fig. 15. The measured result showed positive gains in the entire frequency band of interest. Especially at around 28 GHz, the gain is observed to be higher than 10 and 20 dB at maximum. The LNA, which was flip-chip mounted on the glass-based package, is originally designed by the manufacturer to be wire bonded, where the LNA is faced up. The selection of LNAs designed for flip-chip modules could provide flat gain across the whole band of interest. It is, therefore, reiterated that the codesign of integrated ICs, antennas, and packaging is critical to obtain optimal performance in front-end modules.

V. COMPARISON

The comparisons between the proposed work and the previously reported articles are summarized in Table IV. The parameters associated with the antenna performance are based on a single antenna element. Key substrate technologies (PCB, LTCC, multilayered organic, and glass) with integrated antenna operating at 5G frequency bands are benchmarked for the comparison. As shown in Table IV, the proposed work covers the important frequency bands around 28 GHz (n257, n258, and n261) with the thinnest substrate (100 μm). The relative thickness in the proposed work shown in the table includes the thickness of assembled die (100 μm), the height of the solder resist and multilayers formed on the core substrate, and bump height (50 μm), which results in 300 μm in total (0.028λ_0 at 28 GHz). The proposed work also demonstrated horizontal and vertical interconnects with solder resist patterned for IC assembly.

VI. CONCLUSION

This article presents heterogeneous integration of AiP, seamless or low-loss antenna-to-receiver signal transitions, and flip-chip assembly on panel-scale ultrathin glass substrates, in the 28-GHz band for high-speed 5G communication standards. The key benefits of glass core, such as dimensional stability, thickness control, unique laminated glass stack-up, and via-in-via processes, result in process stability and design flexibility for system design. Module-level characterization results highlight the low interconnect signal losses with a TPV loss of 0.021 dB/TPV at 28 GHz. The Yagi–Uda antenna fabricated on glass substrates showed a center frequency of 25.85 GHz with a fractional bandwidth of 28.2%, which covers the 28-GHz 5G frequency bands of interest. The antenna also featured a wide-angle main lobe at the target frequency range, implying good coverage of signal transmission and reception. Overall, this article reports package-integrated antenna, feedlines, low-loss interconnects, and assembly of

active ICs and discrete passive components implemented with 100-μm glass-substrate technology.

ACKNOWLEDGMENT

The authors would like to thank Taiyo Ink Mfg. Company, Ltd. for supplying solder resist. They also like to acknowledge Ajinomoto for providing low-loss dielectric films and AGC Inc. for supplying glass substrates with drilled through-glass vias. They wish to acknowledge engineers from Qualcomm for their supportive advice on designs. They also would like to acknowledge the Georgia Tech Packaging Research Center consortium members for their support.

REFERENCES

[1] A. H. Aljuhani, T. Kanar, S. Zihir, and G. M. Rebeiz, "A scalable dual-polarized 256-element Ku-band SATCOM phased-array transmitter with 36.5 dBW EIRP per polarization," in *Proc. 48th Eur. Microw. Conf. (EuMC)*, Sep. 2018, pp. 938–941.

[2] T.-H. Lin, P. M. Raj, A. Watanabe, V. Sundaram, R. Tummala, and M. M. Tentzeris, "Nanostructured miniaturized artificial magnetic conductors (AMC) for high-performance antennas in 5G, IoT, and smart skin applications," in *Proc. IEEE 17th Int. Conf. Nanotechnol. (IEEE-NANO)*, Jul. 2017, pp. 911–915.

[3] J. Dunworth *et al.*, "28 GHz phased array transceiver in 28 nm bulk CMOS for 5G prototype user equipment and base stations," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 1330–1333.

[4] X. Gu *et al.*, "Development, implementation, and characterization of a 64-element dual-polarized phased-array antenna module for 28-GHz high-speed data communications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2975–2984, Jul. 2019.

[5] T. Thai, S. Dalmia, J. Hagn, P. Talebbeydokhti, and Y. Tsfati, "Novel multicore PCB and substrate solutions for ultra broadband dual polarized antennas for 5G millimeter wave covering 28 GHz & 39 GHz range," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 954–959.

[6] A. Nafe, M. Sayginer, K. Kibaroglu, and G. M. Rebeiz, "2×64 dual-polarized dual-beam single-aperture 28 GHz phased array with high cross-polarization rejection for 5G polarization MIMO," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 484–487.

[7] A. O. Watanabe *et al.*, "First demonstration of 28 GHz and 39 GHz transmission lines and antennas on glass substrates for 5G modules," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, May 2017, pp. 236–241.

[8] S. Li, T. Chi, J.-S. Park, H. T. Nguyen, and H. Wang, "A 28-GHz flip-chip packaged Chireix transmitter with on-antenna outphasing active load modulation," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1243–1253, May 2019.

[9] W. C. Yang, H. Wang, W. Q. Che, Y. Huang, and J. Wang, "High-gain and low-loss millimeter-wave LTCC antenna array using artificial magnetic conductor structure," *IEEE Trans. Antennas Propag.*, vol. 63, no. 1, pp. 390–395, Jan. 2015.

[10] Y. Li, C. Wang, and Y. X. Guo, "A Ka-band wideband dual-polarized magnetoelectric dipole antenna array on LTCC," *IEEE Trans. Antennas Propag.*, vol. 68, no. 6, pp. 4985–4990, Jun. 2020.

[11] X. Gu, D. Liu, C. Baks, J.-O. Plouchart, W. Lee, and A. Valdes-Garcia, "An enhanced 64-element dual-polarization antenna array package for W-band communication and imaging applications," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 197–201.

[12] M. Wojnowski, C. Wagner, R. Lachner, J. Böck, G. Sommer, and K. Pressel, "A 77-GHz SiGe single-chip four-channel transceiver module with integrated antennas in embedded wafer-level BGA package," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, May 2012, pp. 1027–1032.

[13] C.-W. Hsu, C.-H. Tsai, J.-S. Hsieh, K.-C. Yee, C.-T. Wang, and D. Yu, "High performance chip-partitioned millimeter wave passive devices on smooth and fine pitch InFO RDL," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, May 2017, pp. 254–259.

[14] A. Rashidian, S. Jafarlou, A. Tomkins, K. Law, M. Tazlauanu, and K. Hayashi, "Compact 60 GHz phased-array antennas with enhanced radiation properties in flip-chip BGA packages," *IEEE Trans. Antennas Propag.*, vol. 67, no. 3, pp. 1605–1619, Mar. 2019.

[15] D. Liu, X. Gu, C. W. Baks, and A. Valdes-Garcia, "Antenna-in-Package design considerations for Ka-band 5G communication applications," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6372–6379, Dec. 2017.

[16] A. Bhutani *et al.*, "122 GHz aperture-coupled stacked patch microstrip antenna in LTCC technology," in *Proc. 10th Eur. Conf. Antennas Propag. (EuCAP)*, Apr. 2016, pp. 1–5.

[17] J.-K. Du *et al.*, "Dual-polarized patch array antenna package for 5G communication systems," in *Proc. 11th Eur. Conf. Antennas Propag. (EUCAP)*, Mar. 2017, pp. 3493–3496.

[18] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A scalable 64-element 28 GHz phased-array transceiver with 50 dBm EIRP and 8-12 Gbps 5G link at 300 meters without any calibration," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 496–498.

[19] A. Watanabe *et al.*, "Leading-edge and ultra-thin 3D glass-polymer 5G modules with seamless antenna-to-transceiver signal transmissions," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 2026–2031.

[20] M. Ali, A. Watanabe, T.-H. Lin, M. R. Pulugurtha, M. M. Tentzeris, and R. R. Tummala, "3D glass package-integrated, high-performance power dividing networks for 5G broadband antennas," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 960–967.

[21] T. Kamgaing, A. A. Elsherbini, T. W. Frank, S. N. Oster, and V. R. Rao, "Investigation of a photodefinable glass substrate for millimeter-wave radios on package," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 1610–1615.

[22] S. Hwangbo, Y.-K. Yoon, and A. B. Shorey, "Millimeter-wave wireless chip-to-chip (C2C) communications in 3D system-in-packaging (SiP) using compact through glass via (TGV)-integrated antennas," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 2074–2079.

[23] C. Chang, C. Lin, and W. Cheng, "Fully integrated 60 GHz switched-beam phased antenna array in glass-IPD technology," *Electron. Lett.*, vol. 51, no. 11, pp. 804–806, 2015.

[24] A. H. Naqvi, J. Park, C. Baek, and S. Lim, "Via-monopole based quasi Yagi-Uda antenna for W-band applications using through glass silicon via (TGSV) technology," *IEEE Access*, vol. 8, pp. 9513–9519, 2020.

[25] R. Bowrothu, Y.-K. Yoon, and J. Zhang, "Through glass via (TGV) based band pass filter for 5G communications," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 1097–1102.

[26] A. H. Naqvi, J.-H. Park, C.-W. Baek, and S. Lim, "V-band end-fire radiating planar micromachined helical antenna using through-glass silicon via (TGSV) technology," *IEEE Access*, vol. 7, pp. 87907–87915, 2019.

[27] Y.-H. Chen *et al.*, "20 × 20 panel size glass IPD interposer manufacturing," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, May 2016, pp. 2146–2150.

[28] Y. Sato and N. Kidera, "Demonstration of 28 GHz band pass filter toward 5G using ultra low loss and high accuracy through quartz vias," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 2243–2247.

[29] L. Martin *et al.*, "Attenuation of high frequency signals in structured metallization on glass: Comparing different metallization techniques with 24 GHz, 77 GHz and 100 GHz structures," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 726–732.

[30] K. Hayashi, N. Kidera, and Y. Sato, "Low-loss glass substrates formulated with a variety of dielectric characteristics for millimeter-wave applications," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 712–717.

[31] A. O. Watanabe, B. K. Tehrani, T. Ogawa, P. M. Raj, M. M. Tentzeris, and R. R. Tummala, "Ultralow-loss substrate-integrated waveguides in glass-based substrates for millimeter-wave applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 10, no. 3, pp. 531–533, Mar. 2020.

[32] Y. Uemichi, O. Nukaga, X. Han, R. Hosono, N. Guan, and S. Amakawa, "Characterization of 60-GHz silica-based post-wall waveguide and low-loss substrate dielectric," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, Dec. 2016, pp. 1–4.

[33] R. Bowrothu, S. Hwangbo, T. Schumann, and Y.-K. Yoon, "28 GHz through glass via (TGV) based band pass filter using through fused silica via (TFV) technology," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 695–699.

[34] H.-D. Chang *et al.*, "Development and characterization of new generation panel fan-out (P-FO) packaging technology," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 947–951.

[35] T. Braun *et al.*, "Large area compression molding for fan-out panel level packing," in *Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 1077–1083.
[36] M. Ali *et al.*, "First demonstration of compact, ultra-thin low-pass and bandpass filters for 5G small-cell applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 12, pp. 1110–1112, Dec. 2018.
[37] J. Kim *et al.*, "High-frequency scalable electrical model and analysis of a through silicon via (TSV)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 181–195, Feb. 2011.
[38] I.-J. Hwang, H.-W. Jo, J.-W. Kim, G. Kim, J.-W. Yu, and W.-W. Lee, "Vertically stacked folded dipole antenna using multi-layer for mm-wave mobile terminals," in *Proc. IEEE Int. Symp. Antennas Propag., USNC/URSI Nat. Radio Sci. Meeting*, Jul. 2017, pp. 2579–2580.
[39] W. El-Halwagy, R. Mirzavand, J. Melzer, M. Hossain, and P. Mousavi, "Investigation of wideband substrate-integrated vertically-polarized electric dipole antenna and arrays for mm-wave 5G mobile devices," *IEEE Access*, vol. 6, pp. 2145–2157, 2018.
[40] G. Guo, L.-S. Wu, Y.-P. Zhang, and J.-F. Mao, "Stacked patch array in LTCC for 28 GHz antenna-in-package applications," in *Proc. IEEE Electr. Design Adv. Packag. Syst. Symp. (EDAPS)*, Dec. 2017, pp. 1–3.
[41] H. Xia, T. Zhang, L. Li, and F. Zheng, "A 1×2 taper slot antenna array with flip-chip interconnect via glass-IPD technology for 60 GHz radar sensors," *IEEE Access*, vol. 8, pp. 61790–61796, 2020.
[42] Analog Devices. *HMC-ALH369-DIE*. Accessed: Jun. 2020. [Online]. Available: https://www.analog.com/en/products/hmc-alh369-die.html#product-overview

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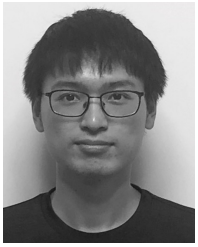

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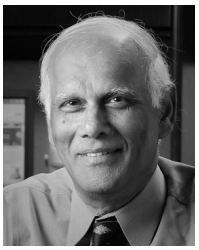

Rao R. Tummala (Life Fellow, IEEE) was an IBM Fellow and the Director of the Advanced Packaging Lab (APTL) in 1993 pioneering such major technologies as the industry's first plasma display in the 1970s and, the first and next two generations of 100-chip MCM package integration, now called chiplet MCMs, in the 1980s for servers, mainframes, and supercomputers. He is currently a Distinguished and Endowed Chair Professor and the Director Emeritus with Georgia Tech, Atlanta, GA, USA. He is well known as an industrial technologist, a technology pioneer, and an educator. He is the Father of the System-on-Package (SOP) concept versus System-on-chip (SOC) by the industry. He has been a consultant and an advisor to many of Fortune 500 semiconductor and systems companies. As an educator, he was instrumental in setting up the largest and most comprehensive Academic Center funded by NSF as the first and only the NSF Engineering Research Center in Electronic Systems Packaging at Georgia Tech. Such a center, under his leadership, pioneered an integrated approach to research, education, and global industry collaborations. It involved about 30 academic and full-time research faculty, 200 Ph.D. and M.S. students, and 50–70 industry and academic collaborators from USA, Europe, Japan, Korea, India, and Taiwan. It educated thousands of engineers in packaging in classrooms and hands-on labs and produced more than 1000 engineers with Ph.D., M.S., and B.S. degrees. He has published about 800 technical articles and invented technologies that resulted in over 110 patents and inventions. He wrote the first modern handbook in packaging, *Microelectronics Packaging Handbook* (McGraw-Hill, 1988); then first undergrad textbook, *Fundamentals of Microsystem Packaging* (2001); and the first book introducing the concept of SOP, *Introduction to System-on-Package* (2006) and *Fundamentals of Device and Systems Packaging* (Second Edition, 2020).

Dr. Tummala is a member of the National Academy of Engineering and a Fellow of the International Microelectronic & Packaging Society (IMAPS) and the American Ceramic Society. He received more than 50 industry, academic and professional society awards, including 12 invention and four corporate awards from IBM, the IEEE Award David Sarnoff Award for Industry's First MCM in 1991, the ASM-International's Engineering Materials Achievement Award for LTCC in 1992, the IEEE CPMT's Sustained Technical Achievement Award in 1992, the European Electronic Materials Award from DVM in 1995, the Dan Hughes Award from IMAPS in 1997, the John Jeppson Award from the American Ceramic Society in 1998, the John A. Wagnon's Award from IMAPS in 1998, named by US News and World Report as one of the 50 Stars in US for US competitiveness in 1999, the Total Excellence in Manufacturing Award from ASE in 2000, the Educator of the Year for Excellence in Teaching, Research, and Innovation in Electronics from the India-America Cultural Association in 2002, and the Techno-visionary Award from the Semiconductor Industry Association of India in 2010. He is also a Distinguished Alumni of the Indian Institute of Science, Bengaluru, India, in 2000, and the University of Illinois in 1988, and a Distinguished Faculty of Georgia Tech in 2002. He was the President of the IEEE CPMT and IMAPS societies.

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Dr. Swaminathan is also the Founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the EPS Society. He has served as the Distinguished Lecturer for the IEEE EMC Society.